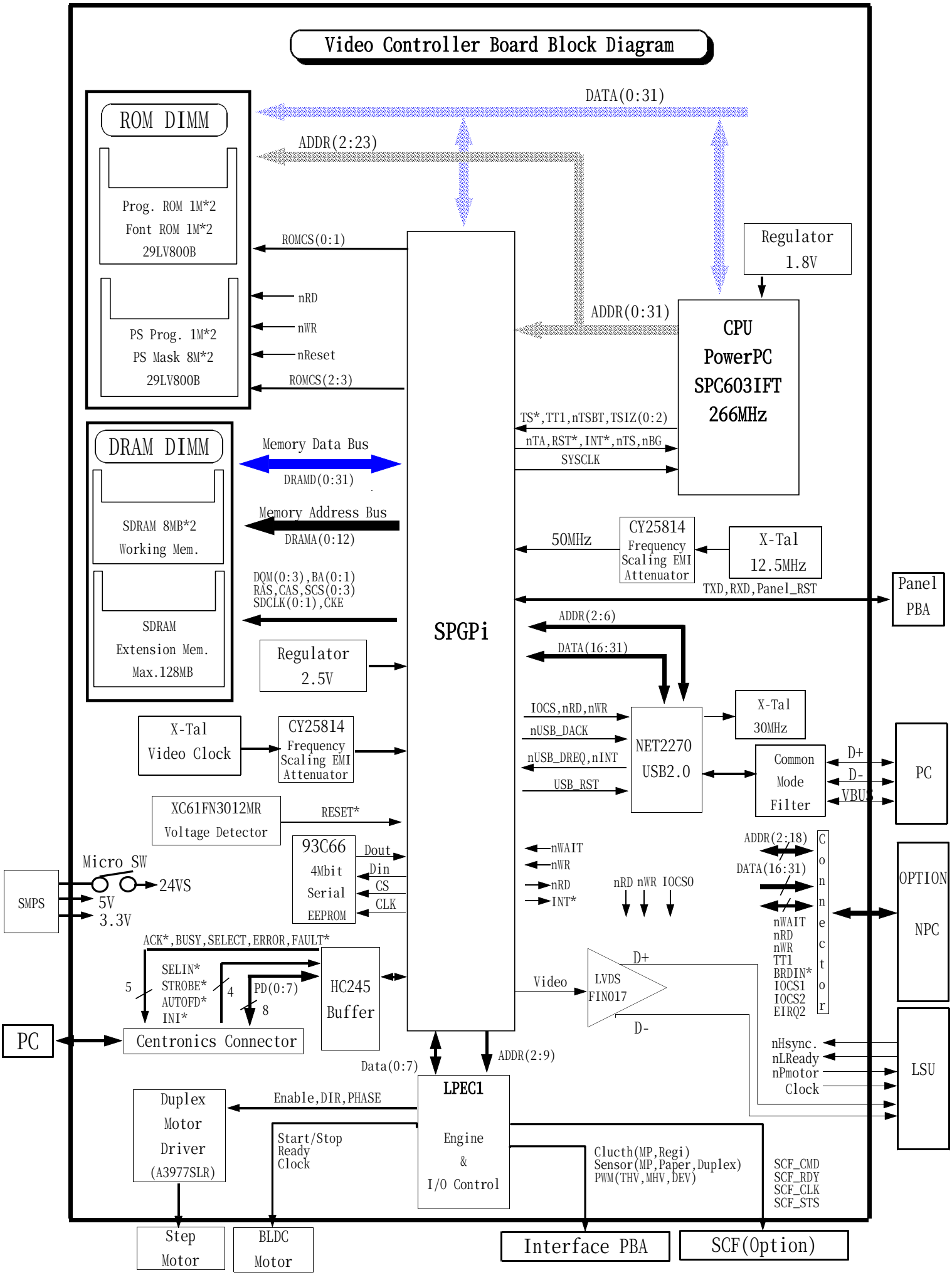
Video Controller Board Block Diagram
ROM DIMM
Prog. ROM 1M*2
Font ROM 1M*2
29LV800B
PS Prog. 1M*2
PS Mask 8M*2
29LV800B
DRAM DIMM
SDRAM 8MB*2
Working Mem.
SDRAM
Extension Mem.
Max.128MB
DATA(0:31)
ADDR(2:23)
ROMCS(0:1)
nRD
nWR
nReset
ROMCS(2:3)
Memory Data Bus
DRAMD(0:31)
Memory Address Bus
DRAMA(0:12)
DQM(0:3),BA(0:1)
RAS,CAS,SCS(0:3)
SDCLK(0:1),CKE
Regulator
2.5V
SPGPi
Regulator
1.8V
ADDR(0:31)
CPU
PowerPC
SPC603IFT
266MHz
TS*,TT1,nTSBT,TSIZ(0:2)
nTA,RST*,INT*,nTS,nBG
SYSCLK
50MHz
CY25814
Frequency
Scaling EMI
Attenuator
X-Tal
12.5MHz
TXD,RXD,Panel_RST
Panel
PBA
ADDR(2:6)
DATA(16:31)
IOCS,nRD,nWR
nUSB_DACK
nUSB_DREQ,nINT
USB_RST
NET2270
USB2.0
X-Tal
30MHz
Common
Mode
Filter
D+
D-
VBUS
PC
X-Tal
Video Clock
CY25814
Frequency
Scaling EMI
Attenuator
XC61FN3012MR
Voltage Detector
RESET*
93C66
4Mbit
Serial
EEPROM
Dout
Din
CS
CLK
nWAIT
nWR
nRD
INT*
nRD nWR IOCS0
ADDR(2:18)
DATA(16:31)
Connector
nWAIT
nRD
nWR
TT1
BRDIN*
IOCS1
IOCS2
EIRQ2
OPTION
NPC
Micro SW
24VS
SMPS
5V
3.3V
ACK*,BUSY,SELECT,ERROR,FAULT*
SELIN*
STROBE*
AUTOFD*
INI*
5
4
PD(0:7)
8
HC245
Buffer
Video
LVDS
FIN017
D+
D-
PC
Centronics Connector
Data(0:7)
ADDR(2:9)
LPEC1
Engine
&
I/O Control
nHsync.
nLReady
nPmotor
Clock
LSU
Duplex
Motor
Driver
(A3977SLR)
Enable,DIR,PHASE
Start/Stop
Ready
Clock
Clucth(MP,Regi)
Sensor(MP,Paper,Duplex)
PWM(THV,MHV,DEV)
SCF_CMD
SCF_RDY
SCF_CLK
SCF_STS
Step
Motor
BLDC
Motor
Interface PBA
SCF(Option)