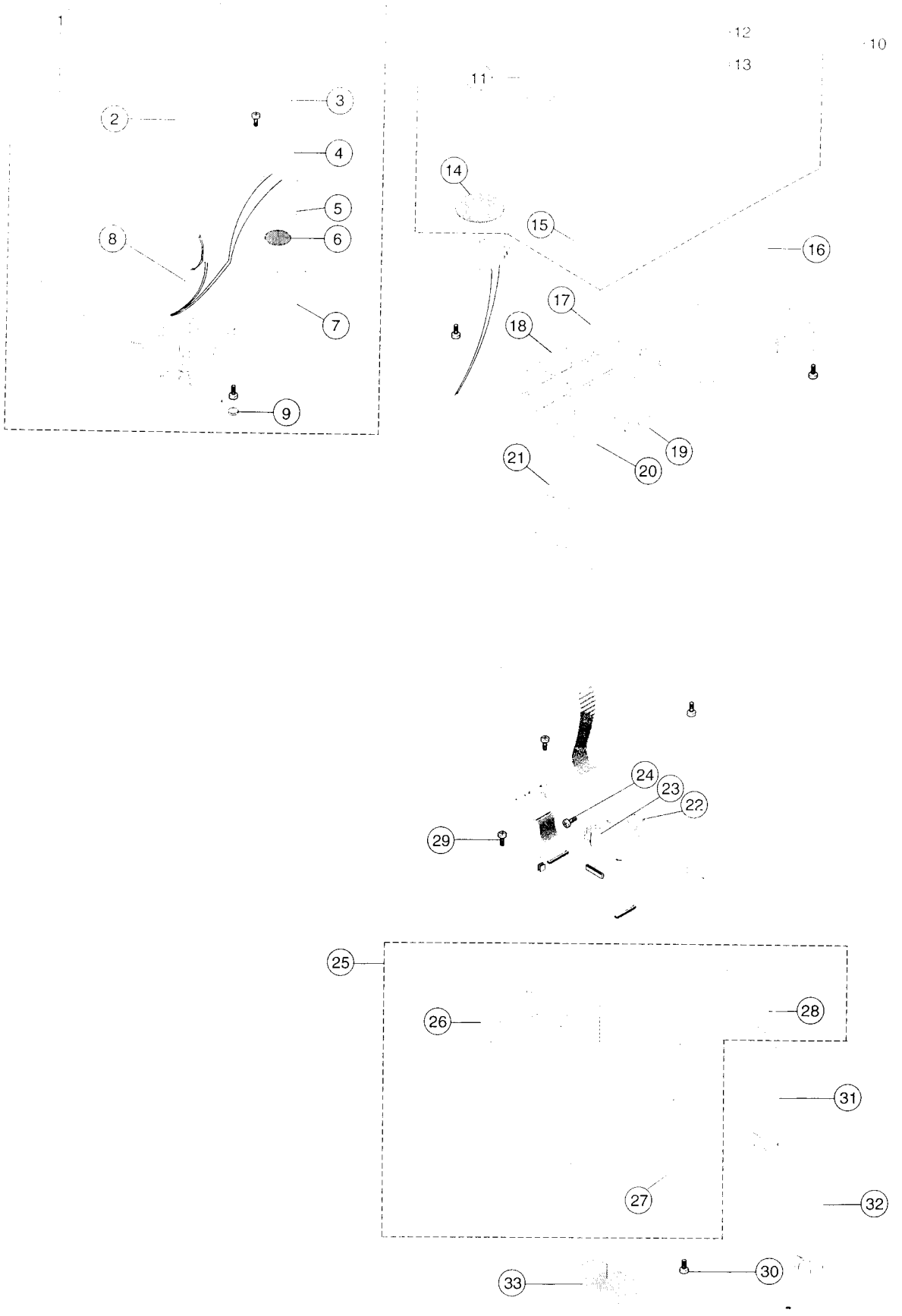
7. Exploded View and its Parts List

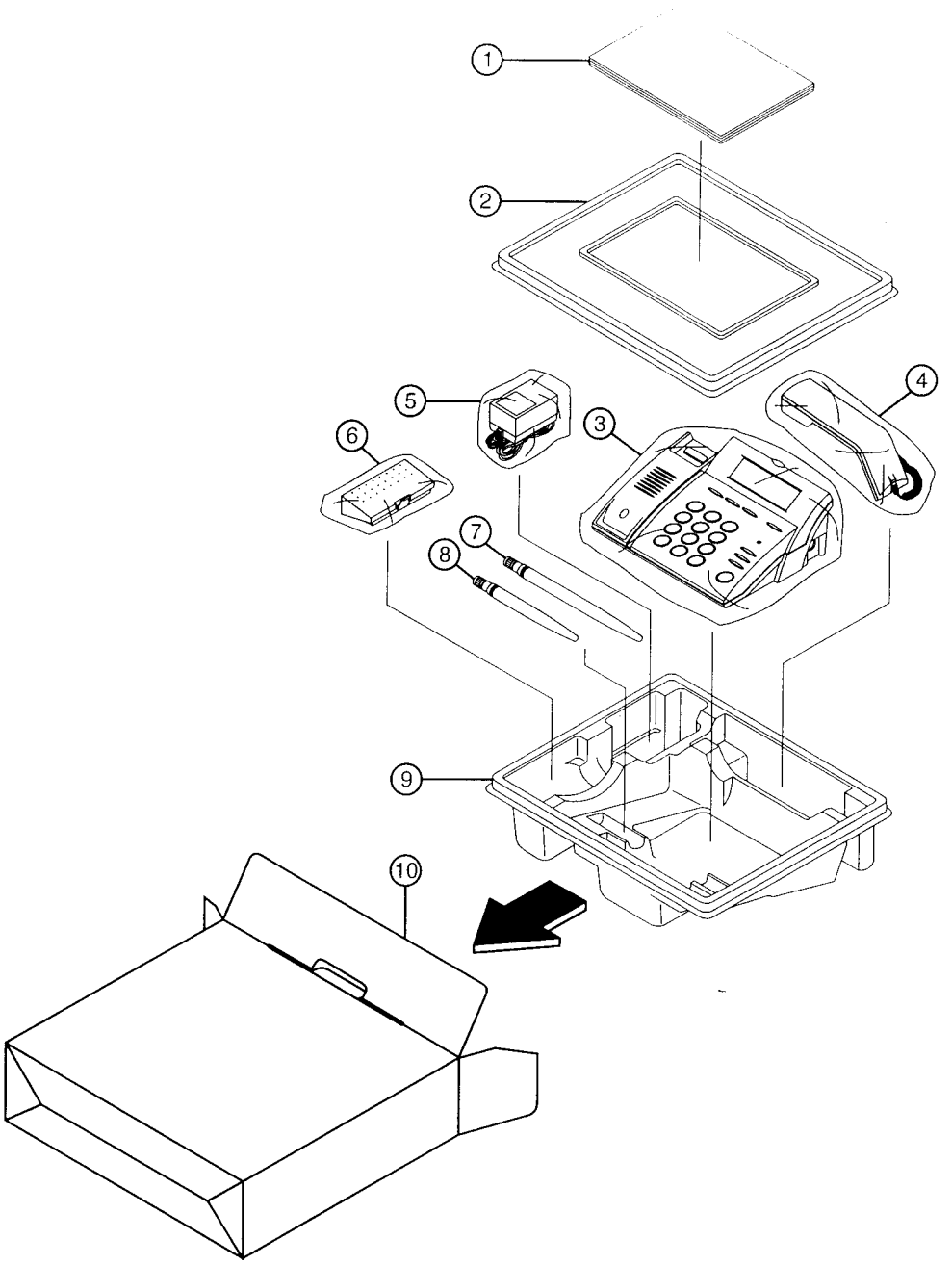
7-1 Fixed Phone Exploded View



7-2 Fixed Phone Parts List

NO	DESCRIPTION	SEC. CODE	Q'TY	REMARK
1	Handset Assy'	GH96-01089A	1	
2	Handset Upper	GH72-41447A	1	
3	Sponge Unit	GH74-10586A	1	
4	WEIGHT BALANCE	GH70-10629A	1	
5	SPONG BUMPER	GG74-10587A	1	
6	FELT SPEAKER	GG74-10648A	1	
7	HANDSET LOWER	GH72-41448A	1	
8	MIC HOLDER	GG73-40549A	1	
9	HOLE DUMMY	GH73-40665A	1	
10	SUA, LIPPER HOUSING	GH75-11151A	1	
11	UPPER-HOUSING	GH72-41445A	1	
12	POWER-LED	GH72-41462A	1	
13	REFLECTOR-LED	GG72-41461A	1	
14	SPONGE SPEAKER	GH74-10502B	1	
15	PLUNGER	GH72-41449A	1	
16	WINDOW-LCD	GH72-41463A	1	
17	4 FUNCTION KEY	GH72-41466A	1	
18	3 × 4 FUNCTION KEY	GH72-41467A	1	
19	3 FUNCTION KEY	GH72-41465A	1	
20	ON/HOOK KEY	GH72-41467A	1	
21	KEY RUBBER	GH73-40662A	1	
22	SUA, CONTACT BATTERY	GH75-11152A	1	
23	HEAT SINK	GH62-30001A	1	
24	SCREW MACHINE	6001-000571	5	
25	SUA, LOWER HOUSING	GH96-01284A	1	
26	LOWER HOUSING	GH72-41446A	1	
27	FOOT-RUBBER	GH73-40663A	4	
28	COVER-BATTERY	GH72-41468A	1	
29	SCREW TAPTITE	6003-000108	30	
29	SCREW TAPTITE	6003-000109	5	
29	ANTENA	GH42-10516A	1	SCW-F2000
29	ANTENA	GH42-10517A	1	SCW-F200
33	LABEL ID MAIN	GH68-31051A	1	ENGLISH

7-3 Main Packing Layout



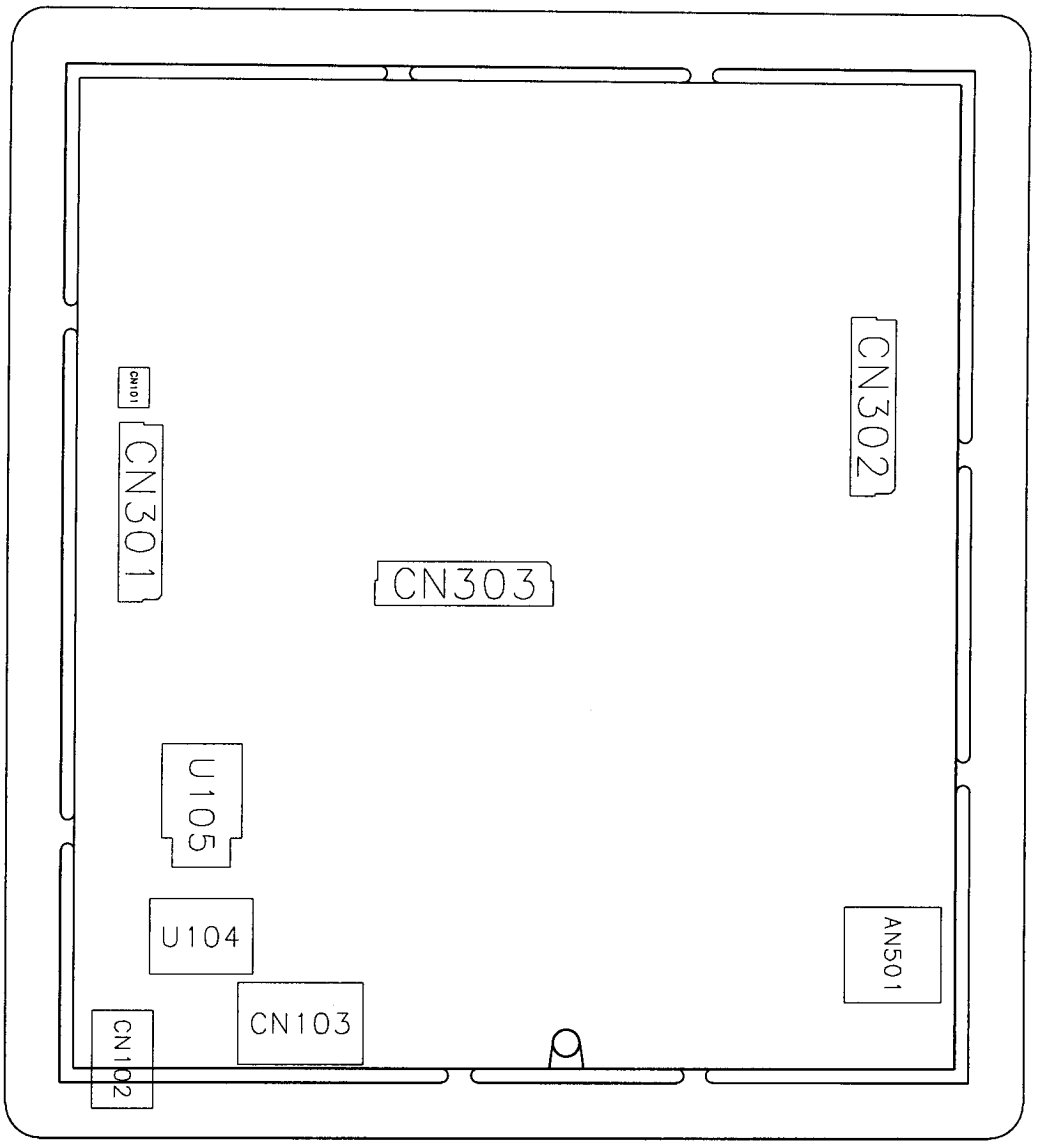
7-4 Main Packing Parts List

NO	DESCRIPTION	SEC. CODE	Q'TY	REMARK
1	USER MANUAL		1	ENGLISH
2	CUSION COVER-MAIN	GG69-20670A	1	
3	MAIN ASSY'	GH97-01285A	1	
4	HANDSET ASSY'	GH96-01089A	1	
5	ADAPTER		1	
6	BATTERY ASSY'	GH43-10105A	1	
7	ANTENA	GH42-10517A	1	SCW-F200
8	ANTENA	GH42-10516A	1	SCW-F2000
9	CUSION CASE-MAIN	GG69-20671A	1	
10	BOX GIFT-MAIN	GH69-11138A	1	

MEMO

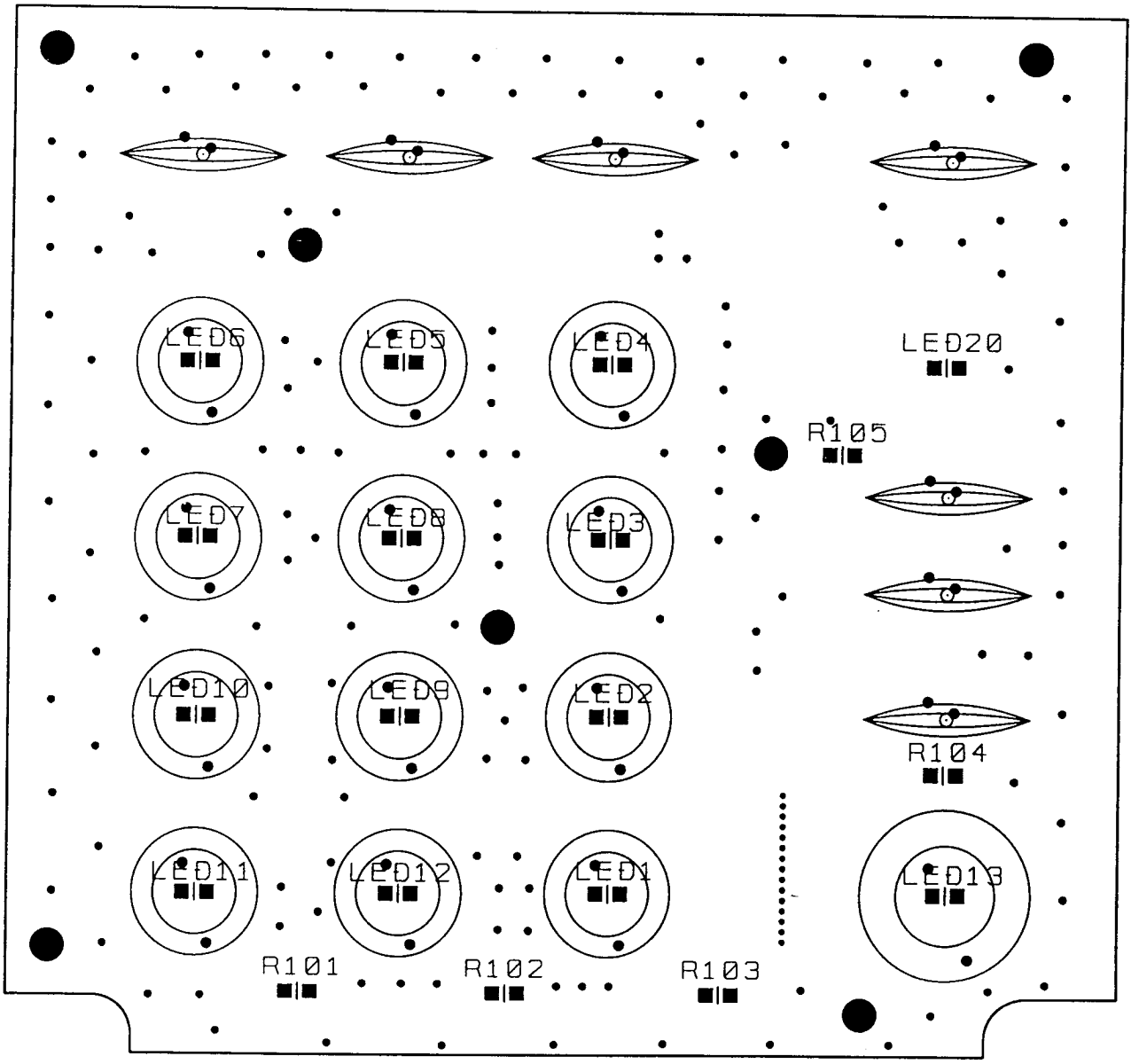
8. PCB Diagrams

U304
U113
U301
U302
U114
U112
U102
U109
U303
OSC502
U701
F503
U503
C701
U702
U703
U505
OSC501
F501
U707
U708
C135
C134
D104
D103

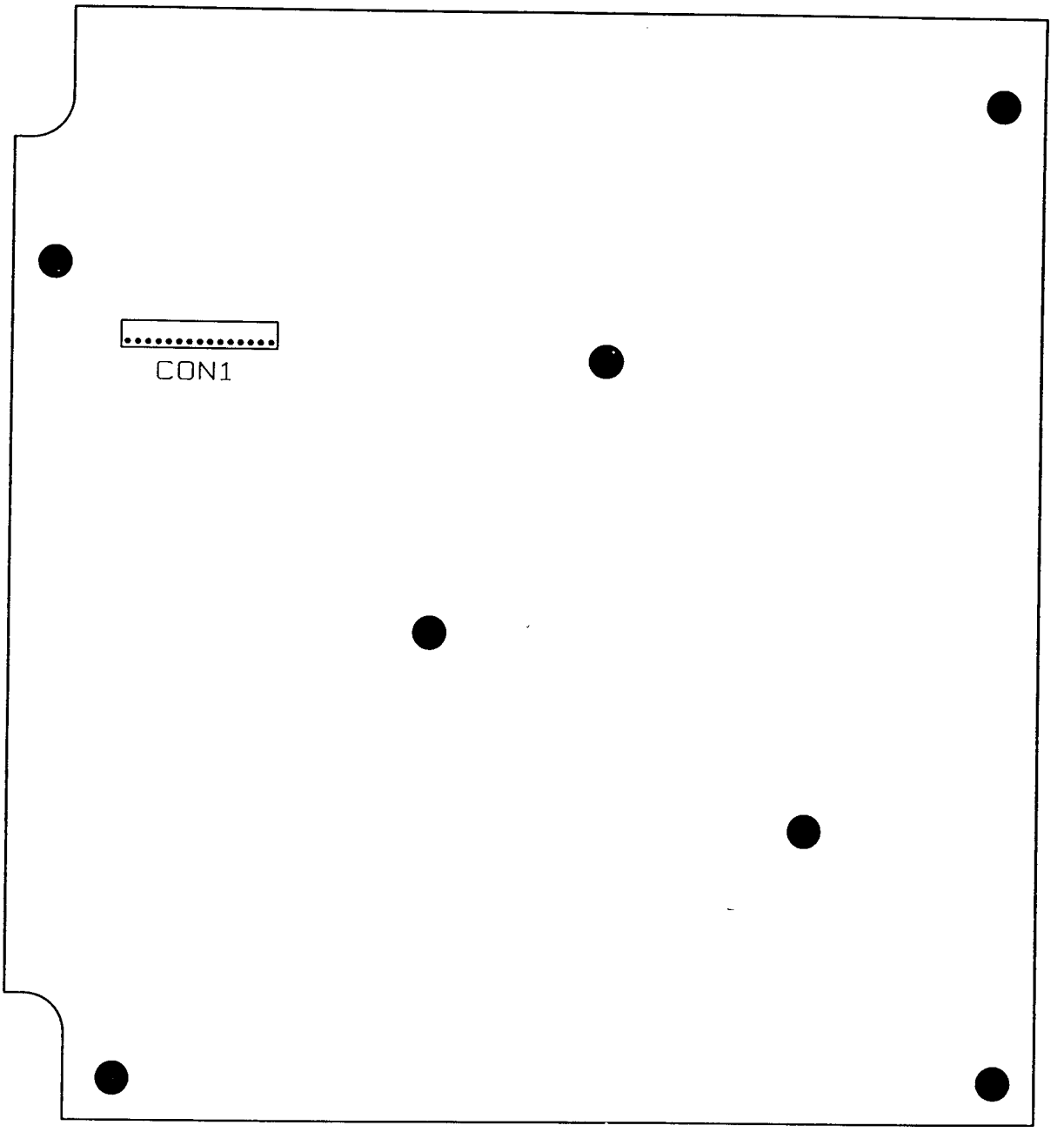

CN101
CN301
CN302
CN303
U105
U104
AN501
CN103
CN102

8-2 Keypad

Top View

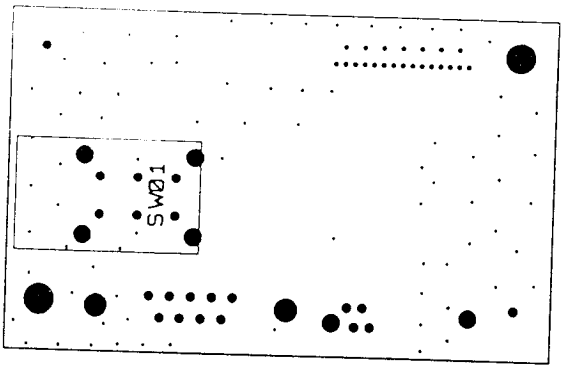


Bottom View

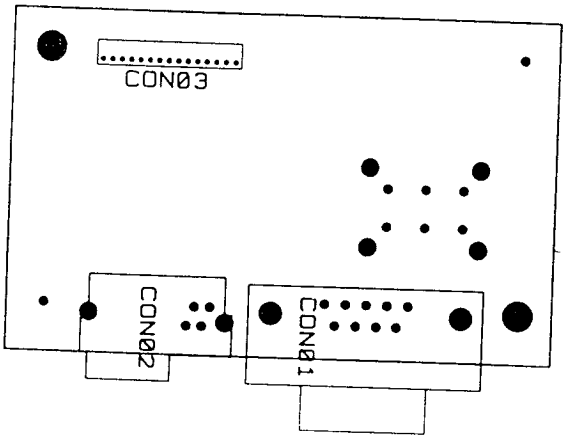


8-3 Hook Board

Top View



Bottom View



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9. Electrical Parts List

9. Electrical Parts List

NO	DESCRIPTION		SEC. CODE	REMARK
	- Capacitors -			
AN501	BNC, JACK, 3mohm, 50ohm	HIROSE	3705-001141	
C101	Ceramic, Chip, 10NF,16V	MURATA	2203-000254	
C102	Ceramic, Chip, 8.2NF,16V	MURATA	2203-001210	
C103	Ceramic, Chip, 8.2NF,16V	MURATA	2203-001210	
C104	Ceramic, Chip, 220PF,16V	MURATA	2203-000585	
C105	Ceramic,Chip, 10NF,16V	MURATA	2203-000254	
C106	Ceramic, Chip, 1NF,50V	MURATA	2203-000438	
C107	Ceramic, Chip, 100NF,25V	MURATA	2203-000189	
C108	Tantalum,Chip,10UF,6.3V	AVX	2404-000139	
C112	Ceramic, Chip, 100NF,25V	MURATA	2203-000189	
C113	Ceramic, Chip, 100NF,25V	MURATA	2203-000189	
C114	Ceramic, Chip, 100NF,25V	MURATA	2203-000189	
C132	Ceramic, Chip, 100NF,25V	MURATA	2203-000189	
C133	Ceramic, Chip, 10NF,16V	MURATA	2203-000254	
C134	Tantalum, Chip, 22UF,16V	AVX	2404-000189	
C135	Tantalum, Chip, 33UF,16V	AVX	2404-000222	
C136	Tantalum, Chip, 1UF,16V	AVX	2404-000151	
C137	Ceramic, Chip, 8.2NF,16V	MURATA	2203-001210	
C138	Ceramic, Chip, 8.2NF,16V	MURATA	2203-001210	
C139	Ceramic, Chip, 100NF,25V	MURATA	2203-000189	
C140	Ceramic, Chip, 100NF,25V	MURATA	2203-000189	
C141	Tantalum, Chip, 10UF,6.3V	AVX	2404-000139	
C142	Ceramic, Chip, 100NF,25V	MURATA	2203-000189	
C143	Tantalum, Chip, 10UF,6.3V	AVX	2404-000139	
C144	Ceramic, Chip, 68PF,50V	MURATA	2203-001153	

NO	DESCRIPTION		SEC. CODE	REMARK
C145	Ceramic, Chip, 68PF,50V	MURATA	2203-001153	
C146	Ceramic, Chip, 100NF,25V	MURATA	2203-000189	
C147	Ceramic, Chip, 100NF,25V	MURATA	2203-000189	
C148	Ceramic, Chip, 10NF,16V	MURATA	2203-000254	
C149	Ceramic, Chip, 100NF,25V	MURATA	2203-000189	
C150	NC	OPEN		
C151	Ceramic, Chip, 10NF,16V	MURATA	2203-000254	
C152	Ceramic, Chip, 100NF,25V	MURATA	2203-000189	
C153	Ceramic, Chip, 10NF,16V	MURATA	2203-000254	
C154	Ceramic, Chip, 100NF,25V	MURATA	2203-000189	
C155	Ceramic, Chip, 10NF,16V	MURATA	2203-000254	
C156	Ceramic, Chip, 100NF,25V	MURATA	2203-000189	
C157	Ceramic, Chip, 10NF,16V	MURATA	2203-000254	
C158	Ceramic, Chip, 470PF,50V	MURATA	2203-000941	
C159	Ceramic, Chip, 100PF,50V	MURATA	2203-000234	
C161	Ceramic, Chip, 5PF,50V	MURATA	2203-001437	
C162	Ceramic, Chip, 5PF,50V	MURATA	2203-001437	
C163	Ceramic, Chip, 100NF,25V	MURATA	2203-000189	
C164	Ceramic, Chip, 100NF,25V	MURATA	2203-000189	
C165	Ceramic, Chip, 100NF,25V	MURATA	2203-000189	
C166	Ceramic, Chip, 100NF,25V	MURATA	2203-000189	
C167	Tantalum, Chip, 10UF,6.3V	AVX	2404-000139	
C168	Ceramic, Chip, 100NF,25V	MURATA	2203-000189	
C301	NC	OPEN		
C302	Ceramic, Chip, 100NF,25V	MURATA	2203-000189	
C303	Ceramic, Chip, 100NF,25V	MURATA	2203-000189	

NO	DESCRIPTION		SEC. CODE	REMARK
C304	Ceramic, Chip, 100NF,25V	MURATA	2203-000189	
C305	Ceramic, Chip, 10NF,16V	MURATA	2203-000254	
C306	Ceramic, Chip, 10NF,16V	MURATA	2203-000254	
C307	Ceramic, Chip, 100NF,25V	MURATA	2203-000189	
C308	Ceramic, Chip, 2.2NF,50V	MURATA	2203-000489	
C309	Tantalum, Chip, 0.47UF,16V	AVX	2404-000312	
C310	Tantalum, Chip, 0.47UF,16V	AVX	2404-000312	
C311	Tantalum, Chip, 0.47UF,16V	AVX	2404-000312	
C312	Tantalum, Chip, 0.47UF,16V	AVX	2404-000312	
C313	Tantalum, Chip, 0.47UF,16V	AVX	2404-000312	
C314	Tantalum, Chip, 1UF,10V	AVX	2404-000291	
C315	Ceramic, Chip, 100NF,25V	MURATA	2203-000189	
C316	Ceramic, Chip, 100NF,25V	MURATA	2203-000189	
C317	Ceramic, Chip, 100NF,25V	MURATA	2203-000189	
C501	Ceramic, Chip, 10NF,16V	MURATA	2203-000254	
C502	Tantalum, Chip, 4.7UF,10V	AVX	2404-000232	
C503	Ceramic, Chip 10NF,16V	MURATA	2203-000585	
C504	Ceramic, Chip 10NF,16V	MURATA	2203-000254	
C505	Ceramic, Chip 10NF,16V	MURATA	2203-000254	
C506	Tantalum, Chip 4.7UF,10V	AVX	2404-000232	
C507	Tantalum, Chip 4.7UF,10V	AVX	2404-000232	
C508	Ceramic, Chip 470PF,50V	MURATA	2203-000941	
C509	Ceramic, Chip 100PF,50V	MURATA	2203-000234	
C511	Ceramic, Chip 15PF,50V	MURATA	2203-000386	
C512	NC	OPEN		
C513	NC	OPEN		
C514	Ceramic, Chip 100PF,50V	MURATA	2203-000234	

NO	DESCRIPTION		SEC. CODE	REMARK
C515	Ceramic, Chip 100PF,50V	MURATA	2203-000234	
C516	NC	OPEN		
C517	Ceramic, Chip 3PF,50V	MURATA	2203-000870	
C518	Ceramic, Chip 100PF,50V	MURATA	2203-000234	
C519	Ceramic, Chip 100PF,50V	MURATA	2203-000234	
C520	Ceramic, Chip 100PF,50V	MURATA	2203-000234	
C521	Ceramic, Chip 1NF,50V	MURATA	2203-000438	
C522	Ceramic, Chip 0.5PF,50V	MURATA	2203-001383	
C523	Ceramic, Chip 100PF,50V	MURATA	2203-000234	
C524	Ceramic, Chip 1NF,50V	MURATA	2203-000438	
C525	Ceramic, Chip 100PF,50V	MURATA	2203-000234	
C526	Ceramic, Chip 9PF,50V	MURATA	2203-001283	
C527	Ceramic, Chip 1NF,50V	MURATA	2203-000438	
C528	Ceramic, Chip 1NF,50V	MURATA	2203-000438	
C529	Ceramic, Chip 100PF,50V	MURATA	2203-000234	
C530	Ceramic, Chip 1NF,50V	MURATA	2203-000438	
C531	NC	OPEN		
C532	Ceramic, Chip 1NF,50V	MURATA	2203-000438	
C533	Ceramic, Chip 10PF,50V	MURATA	2203-000278	
C534	Ceramic, Chip 4PF,50V	MURATA	2203-001017	
C535	Ceramic, Chip 4PF,50V	MURATA	2203-001017	
C536	Ceramic, Chip 470PF,50V	MURATA	2203-000941	
C537	Tantalum, Chip 4.7UF,10V	AVX	2404-000232	
C538	Ceramic, Chip 47NF,16V	MURATA	2203-001432	
C539	Ceramic, Chip 1PF,50V	MURATA	2203-000466	
C541	Ceramic, Chip 100PF,50V	MURATA	2203-000234	
C542	Ceramic, Chip 1PF,50V	MURATA	2203-000466	

NO	DESCRIPTION		SEC. CODE	REMARK
C543	Ceramic, Chip 100PF,50V	MURATA	2203-000234	
C544	Ceramic, Chip 1NF,50V	MURATA	2203-000438	
C545	Ceramic, Chip 1NF,50V	MURATA	2203-000438	
C546	Ceramic, Chip 10NF,16V	MURATA	2203-000585	
C547	Ceramic, Chip 100PF,50V	MURATA	2203-000234	
C548	Ceramic, Chip 1PF,50V	MURATA	2203-000466	
C549	Ceramic, Chip 1PF,50V	MURATA	2203-000466	
C550	Ceramic, Chip 100PF,50V	MURATA	2203-000234	
C551	Ceramic, Chip 10NF,16V	MURATA	2203-000254	
C552	Ceramic, Chip 100PF,50V	MURATA	2203-000234	
C553	Ceramic, Chip 10NF,16V	MURATA	2203-000254	
C554	Ceramic, Chip 100PF,50V	MURATA	2203-000234	
C555	Tantalum, Chip 4.7UF,10V	AVX	2404-000232	
C556	Ceramic, Chip 10NF,16V	MURATA	2203-000254	
C557	Ceramic, Chip 100PF,50V	MURATA	2203-000234	
C558	Ceramic, Chip 1NF,50V	MURATA	2203-000438	
C559	NC	OPEN		
C560	Tantalum,Chip,1UF,16V	AVX	2404-000151	
C561	Ceramic, Chip 100NF,16V	MURATA	2203-005061	
C562	Ceramic, Chip 100PF,50V	MURATA	2203-000234	
C563	Ceramic, Chip 100PF,50V	MURATA	2203-000234	
C564	Ceramic, Chip 4.7NF,25V	MURATA	2203-000885	
C565	Tantalum, Chip 220NF,35V	AVX	2404-000180	
C566	NC	OPEN		
C567	Ceramic, Chip 47NF,16V	MURATA	2203-001432	
C568	Ceramic, Chip 10PF,50V	MURATA	2203-000278	
C569	Ceramic, Chip 100PF,50V	MURATA	2203-000234	

NO	DESCRIPTION		SEC. CODE	REMARK
C571	Ceramic, Chip 10NF,16V	MURATA	2203-000254	
C572	Tantalum, Chip 4.7UF,10V	AVX	2404-000232	
C573	Ceramic, Chip 10NF,16V	MURATA	2203-000254	
C574	Ceramic, Chip 100PF,50V	MURATA	2203-000234	
C575	Ceramic, Chip 10NF,16V	MURATA	2203-000254	
C576	Ceramic, Chip 10NF,16V	MURATA	2203-000254	
C577	Tantalum, Chip 4.7UF,10V	AVX	2404-000232	
C578	Ceramic, Chip 100PF,50V	MURATA	2203-000234	
C579	Ceramic, Chip 100PF,50V	MURATA	2203-000234	
C581	Ceramic, Chip 100PF,50V	MURATA	2203-000234	
C582	Ceramic, Chip 100PF,50V	MURATA	2203-000234	
C583	Ceramic, Chip 1PF,50V	MURATA	2203-000466	
C584	Ceramic, Chip 1NF,50V	MURATA	2203-000438	
C585	Ceramic, Chip 100PF,50V	MURATA	2203-000234	
C701	Tantalum, Chip 100UF,10V	AVX	2404-000278	
C702	Ceramic, Chip 10NF,16V	MURATA	2203-000254	
C703	Ceramic, Chip 1NF,50V	MURATA	2203-000438	
C704	Ceramic, Chip 10NF,16V	MURATA	2203-000254	
C705	Ceramic, Chip 1NF,50V	MURATA	2203-000438	
C706	Ceramic, Chip 10NF,16V	MURATA	2203-000254	
C707	Ceramic, Chip 1NF,50V	MURATA	2203-000438	
C708	Ceramic, Chip 10NF,16V	MURATA	2203-000254	
C709	Ceramic, Chip 1NF,50V	MURATA	2203-000438	
C711	Ceramic, Chip 10NF,16V	MURATA	2203-000254	
C712	Ceramic, Chip 1NF,50V	MURATA	2203-000438	
C713	Ceramic, Chip 10NF,16V	MURATA	2203-000254	
C714	Ceramic, Chip 1NF,50V	MURATA	2203-000438	

NO	DESCRIPTION		SEC. CODE	REMARK
C715	Ceramic, Chip 10NF,16V	MURATA	2203-000254	
C716	Ceramic, Chip 1NF,50V	MURATA	2203-000438	
C717	Ceramic, Chip 10NF,16V	MURATA	2203-000254	
C718	Ceramic, Chip 1NF,50V	MURATA	2203-000438	
C719	Ceramic, Chip 10NF,16V	MURATA	2203-000254	
C720	Ceramic, Chip 100PF,50V	MURATA	2203-000234	
C721	Ceramic, Chip 1NF,50V	MURATA	2203-000438	
C722	Tantalum, Chip, 10UF,6.3V	AVX	2404-000139	
C723	Ceramic, Chip 100PF,50V	MURATA	2203-000234	
C725	Ceramic, Chip 8.2NF,16V	MURATA	2203-001210	
C726	Ceramic, Chip 8.2NF,16V	MURATA	2203-001210	
C727	Ceramic, Chip 10NF,16V	MURATA	2203-000254	
C728	Ceramic, Chip 68PF,50V	MURATA	2203-001153	
C729	Ceramic, Chip 68PF,50V	MURATA	2203-001153	
C730	Ceramic, Chip 5PF, 50V	MURATA	2203-001437	
C731	Ceramic, Chip 10NF,16V	MURATA	2203-000254	
C732	Ceramic, Chip 10NF,16V	MURATA	2203-000254	
C733	NC	OPEN		
C734	Tantalum, Chip, 1UF,10V	AVX	2404-000291	
C735	Ceramic, Chip 1NF,50V	MURATA	2203-000438	
C736	Ceramic, Chip 6PF,50V	MURATA	2203-001178	
C737	Ceramic, Chip 68PF,50V	MURATA	2203-001153	
C738	Ceramic, Chip 68PF,50V	MURATA	2203-001153	
C739	Ceramic, Chip 10NF,16V	MURATA	2203-000254	
C741	Ceramic, Chip 100PF,50V	MURATA	2203-000234	
C742	Ceramic, Chip 100PF,50V	MURATA	2203-000234	
C743	Ceramic, Chip, 100NF,25V	MURATA	2203-000189	

NO	DESCRIPTION		SEC. CODE	REMARK
C744	Ceramic, Chip, 100NF,25V	MURATA	2203-000189	
C745	Ceramic, Chip 1NF,50V	MURATA	2203-000438	
C746	Ceramic, Chip 1NF,50V	MURATA	2203-000438	
C747	Ceramic, Chip 1NF,50V	MURATA	2203-000438	
C748	Ceramic, Chip 1NF,50V	MURATA	2203-000438	
C749	Ceramic, Chip 47NF,16V	MURATA	2203-001432	
C751	Tantalum, Chip, 10UF,6.3V	AVX	2404-000139	
C752	Ceramic, Chip 1NF,50V	MURATA	2203-000438	
C753	Ceramic, Chip 1NF,50V	MURATA	2203-000438	
C754	Ceramic, Chip 1NF,50V	MURATA	2203-000438	
C755	Ceramic, Chip 1NF,50V	MURATA	2203-000438	
C756	Ceramic, Chip 1PF,50V	MURATA	2203-000466	
C757	Ceramic, Chip 10NF,16V	MURATA	2203-000254	
C758	Ceramic, Chip 100PF,50V	MURATA	2203-000234	
C759	Ceramic, Chip 1NF,50V	MURATA	2203-000438	
C760	NC	OPEN		
C761	NC	OPEN		
C762	Ceramic, Chip 47PF,50V	MURATA	2203-000995	
C763	Ceramic, Chip 10PF,50V	MURATA	2203-000278	
C764	Ceramic, Chip 100PF,50V	MURATA	2203-000234	
C765	Ceramic, Chip 47PF,50V	MURATA	2203-000995	
C766	Ceramic, Chip 100PF,50V	MURATA	2203-000234	
C767	Ceramic, Chip 1NF,50V	MURATA	2203-000438	
C768	Ceramic, Chip 3PF,50V	MURATA	2203-000234	
C769	NC	OPEN		
C770	Ceramic, Chip 3PF,50V	MURATA	2203-000234	
C771	Ceramic, Chip 10NF,16V	MURATA	2203-000254	

NO	DESCRIPTION		SEC. CODE	REMARK
C772	Ceramic, Chip 10NF,16V	MURATA	2203-000254	
C773	Tantalum, Chip, 10UF,6.3V	AVX	2404-000139	
C774	Ceramic, Chip 10NF,16V	MURATA	2203-000254	
C775	NC	OPEN		
C776	NC	OPEN		
C777	NC	OPEN		
C778	Ceramic, Chip 10NF,16V	MURATA	2203-000254	
C779	Ceramic, Chip, 100NF,25V	MURATA	2203-000189	
C781	NC	OPEN		
C782	Tantalum, Chip 4.7UF,10V	AVX	2404-000232	
C783	Ceramic, Chip 10NF,16V	MURATA	2203-000254	
C784	Ceramic, Chip 100PF,50V	MURATA	2203-000234	
C785	Ceramic, Chip 100PF,50V	MURATA	2203-000234	
C786	Ceramic, Chip 1NF,50V	MURATA	2203-000438	
	CONNECTOR -			
CN101	ConnectorHeader,2P,2mm,Straight	MOLEX	3711-000827	
CN102	Jack-AC POWER, 2P, 2mm, BLK	SEOULE	3722-000342	
CN103	MEC-CONTACT BATT SUA	HOJIN	GH75-11152A	
CN301	53398-1590	MOLEX	3711-003938	
CN302	53398-1590	MOLEX	3711-003938	
CN303	53398-1590	MOLEX	3711-003938	
	DIODE-			
D103	Diode, Schottky, RB160L-40TE25	ROHM	0404-000115	
D104	Diode, Rectifier, 1SR154-400	ROHM	0402-000309	
D105	Diode, Zener, UDZ6.8B	ROHM	0403-001172	
D106	Diode, Schottky, RB160L-40TE25	ROHM	0404-000115	
D107	Diode Array, DA204U,20V,100mA	ROHM	0407-000127	

NO	DESCRIPTION		SEC. CODE	REMARK
D108	Diode Array, DA204U,20V,100mA	ROHM	0407-000127	
D109	Diode Array, DA204U,20V,100mA	ROHM	0407-000127	
D111	SM05,6V/1mA,300,SOT-23	SEMTECH	0406-001005	
D112	NC	OPEN		
D301	SM05,6V/1mA,300,SOT-23	SEMTECH	0406-001005	
D302	SM05,6V/1mA,300,SOT-23	SEMTECH	0406-001005	
D501	Diode-Pin,RN731V,50V,50mA	ROHM	0409-000108	
D701	Diode, Varactor, 1SV279, 15V,3nA	TOSHIBA	0405-001035	
D702	Diode, Varactor, 1SV279, 15V,3nA	TOSHIBA	0405-001035	
D703	Diode, Varactor, 1SV279, 15V,3nA	TOSHIBA	0405-001035	
D704	Diode, Varactor, 1SV279, 15V,3nA	TOSHIBA	0405-001035	
	FILTER-			
F501	FILTER-DUPLEXER, 881.5MHz, 836.5MHz	MURATA	2909-001004	
F502	FILTER-SAW, 881.5MHz, 869-894M	FUJITSU	2904-001011	
F503	FILTER-SAW, 85.38MHz,17dB	THOMSON	2904-000297	
F701	FILTER-SAW, 836.5MHz, 25MHz	FUJITSU	2904-001012	
F702	FILTER-SAW, 836.5MHz, 25MHz	FUJITSU	2904-001012	
	CORE-			
L501	CORE-FERRITE	MURATA	3301-001105	
	INDUCTOR-			
L502	INDUCTOR-SMD, 22nH, 5%	TOKO	2703-001422	
L503	INDUCTOR-SMD, 27nH, 10%	TOKO	2703-001413	
L504	INDUCTOR-SMD, 15nH, 5%	TOKO	2703-001190	
L505	Ceramic CHIP, 100PF, 50V	MURATA	2203-000236	
L506	INDUCTOR-SMD, 27nH, 10%	TOKO	2703-001413	
L507	INDUCTOR-SMD, 10nH, 5%	TOKO	2703-001040	
L508	INDUCTOR-SMD, 180nH, 5%	TOKO	2703-001043	

NO	DESCRIPTION		SEC. CODE	REMARK
L509	INDUCTOR-SMD, 180nH, 5%	TOKO	2703-001043	
L511	INDUCTOR-SMD, 1.5UH, 10%	COILCRAFT	2703-000104	
L512	NC	OPEN		
L513	INDUCTOR-SMD, 330nH, 10%	TOKO	2703-000195	
L514	INDUCTOR-SMD, 390nH, 10%	TOKO	2703-000261	
L515	INDUCTOR-SMD, 2.7nH, 10%	TOKO	2703-000301	
L516	INDUCTOR-SMD, 2.7nH, 10%	TOKO	2703-000301	
L517	INDUCTOR-SMD, 8.2nH, 10%	TOKO	2703-001167	
L518	INDUCTOR-SMD, 6.8nH, 5%	TOKO	2703-001207	
	CORE-			
L519	CORE-FERRITE, AB	MURATA	3301-001105	
L520	INDUCTOR-SMD, 8.2NH, 10%	TOKO	2703-001167	
L521	CORE-FERRITE, AB	MURATA	3301-001105	
L522	CORE-FERRITE, AB	MURATA	3301-001105	
L523	Ceramic CHIP, 100PF, 50V	MURATA	2203-000236	
L524	NC	OPEN		
L701	CORE-FERRITE, AB	MURATA	3301-001105	
	INDUCTOR-			
L702	INDUCTOR-SMD, 68nH, 10%	CRAFT	2703-000233	
L703	INDUCTOR-SMD, 27nH, 10%	CRAFT	2703-000304	
L704	INDUCTOR-SMD, 100nH, 10%	TDK	2703-000109	
L705	INDUCTOR-SMD, 100nH, 10%	TDK	2703-000109	
L706	CORE-FERRITE, AB	MURATA	3301-001105	
L707	INDUCTOR-SMD, 18nH, 5%	TOKO	2703-001189	
L708	CORE-FERRITE, AB	MURATA	3301-001105	
L709	CORE-FERRITE, AB	MURATA	3301-001105	
L711	INDUCTOR-SMD, 68nH, 5%	TOKO	2703-001425	

NO	DESCRIPTION		SEC. CODE	REMARK
L712	INDUCTOR-SMD, 6.8nH, 5%	TOKO	2703-001207	
L714	CORE-FERRITE, AB	MURATA	3301-001105	
L715	CORE-FERRITE BEAD, AB	MURATA	3301-001120	
OSC101	RESONATOR-CERAMIC, 27MHz	MURATA	2802-001048	
OSC501	OSCILLATOR-VCO, 954MHz	TOWA	2806-001146	
OSC502	OSCILLATOR-VCTCXO,19.68MHz	KYOCERA	2809-001208	
	TR-			
Q102	TR-POWER, 2SB798, PNP, 2W	NEC	0502-000479	
Q103	FET-GAAS, MGSF3441V, 30V	MOTOROLA	0505-001121	
Q104	TR-Small Signal, MMBT2222A	MOTOROLA	0501-000457	
Q105	FET-GAAS, MGSF3441V	MOTOROLA	0505-001121	
Q106	TR-Small Signal, 2SC4081	ROHM	0501-000218	
Q107	TR-Small Signal, MMBT2222A	MOTOROLA	0501-000457	
Q108	TR-Digital, RN1104	TOSHIBA	0504-000168	
Q109	TR-Digital, RN2104	TOSHIBA	0504-000172	
Q111	TR-Digital, RN1104	TOSHIBA	0504-000168	
Q112	TR-Digital, RN2104	TOSHIBA	0504-000172	
Q113	TR-POWER, 2SB798	NEC	0502-000479	
Q114	TR-Small Signal, MMBT2222A	MOTOROLA	0501-000457	
Q115	TR-Small Signal, MMBT2222A	MOTOROLA	0501-000457	
Q301	TR-Small Signal, MMBT2222A	MOTOROLA	0501-000457	
Q302	TR-Small Signal, 2SC4081	ROHM	0501-000218	
Q303	TR-Small Signal, 2SC4081	ROHM	0501-000218	
Q304	TR-POWER, 2SB798	NEC	0502-000479	
Q305	TR-Small Signal, 2SC4081	ROHM	0501-000218	
Q501	TR-Small Signal, 2SC4081	ROHM	0501-000218	
Q502	FET-SILICON, 2SK2685,P,6V	HITACHI	0505-00111	

NO	DESCRIPTION		SEC. CODE	REMARK
Q503	TR-Small Signal, AT32033	HP	0501-002110	
Q701	TR-Small Signal, 2SC4081	ROHM	0501-000218	
Q702	NC	OPEN		
Q703	FET-GAAS, MGSF3441V, 30V	MOTOROLA	0505-001121	
	REGISTER-			
R101	R-Chip, 4.7Kohm, 5%, 1005	ROHM	2007-000143	
R102	R-Chip, 20Kohm, 5%, 1005	ROHM	2007-000152	
R103	R-Chip, 20Kohm, 5%, 1005	ROHM	2007-000152	
R104	R-Chip, 47Kohm, 5%, 1005	ROHM	2007-000157	
R105	R-Chip, 47Kohm, 5%, 1005	ROHM	2007-000157	
R106	R-Chip, 470ohm, 5%, 1005	ROHM	2007-000932	
R107	R-Chip, 1Kohm, 5%, 1005	ROHM	2007-000140	
R109	R-Chip, 4.7Kohm, 5%, 1005	ROHM	2007-000143	
R110	R-Chip, 1.2Kohm, 5%, 1005	ROHM	2007-001319	
R111	NC	OPEN		
R112	R-Chip, 15ohm, 5%, 1608	ROHM	2007-000416	
R113	R-Chip, 15ohm, 5%, 1608	ROHM	2007-000416	
R114	R-Chip, 1.2Kohm, 5%, 1005	ROHM	2007-001319	
R115	R-Chip, 1.2Kohm, 5%, 1005	ROHM	2007-001319	
R116	R-Chip, 15ohm, 5%, 1005	MATSUSHITA	2007-002965	
R117	R-Chip, 10Kohm, 5%, 1005	ROHM	2007-000148	
R118	R-Chip, 15ohm, 5%, 1608	ROHM	2007-000416	
R126	R-Chip, 10Kohm, 5%, 1005	ROHM	2007-000148	
R127	R-Chip, 1.8Kohm, 5%, 1005	ROHM	2007-001320	
R128	R-Chip, 560ohm, 5%, 1005	ROHM	2007-002797	
R129	R-Chip, 24ohm, 5%, 3216	ROHM	2007-000619	
R131	R-Chip, 24ohm, 5%, 3216	ROHM	2007-000619	

NO	DESCRIPTION		SEC. CODE	REMARK
R132	R-Chip, 1Mohm, 5%, 1005	ROHM	2007-000170	
R133	R-Chip, 200Kohm, 5%, 1608	ROHM	2007-000105	
R134	R-Chip, 10Mohm, 5%, 1608	ROHM	2007-000305	
R135	R-Chip, 15Kohm, 5%, 1005	ROHM	2007-000151	
R136	R-Chip, 200Kohm, 5%, 1608	ROHM	2007-000105	
R137	R-Chip, 100Kohm, 5%, 1005	ROHM	2007-000162	
R138	R-Chip, 10Kohm, 5%, 1005	ROHM	2007-000148	
R139	R-Chip, 100Kohm, 5%, 1005	ROHM	2007-000162	
R141	R-Chip, 20Kohm, 5%, 1005	ROHM	2007-000152	
R142	R-Chip, 20Kohm, 5%, 1005	ROHM	2007-000152	
R143	R-Chip, 20Kohm, 5%, 1005	ROHM	2007-000152	
R144	R-Chip, 20Kohm, 5%, 1005	ROHM	2007-000152	
R146	R-Chip, 270Kohm, 5%, 1005	ROHM	2007-000636	
R147	R-Chip, 150Kohm, 5%, 1005	ROHM	2007-000164	
R148	R-Chip, 82Kohm, 5%, 1005	ROHM	2007-000161	
R149	R-Chip, 82Kohm, 5%, 1005	ROHM	2007-000161	
R150	R-Chip, 10Kohm, 5%, 1005	ROHM	2007-000148	
R151	R-Chip, 15Kohm, 5%, 1005	ROHM	2007-000151	
R152	R-Chip, 1Kohm, 5%, 1005	ROHM	2007-000140	
R153	R-Chip, 22Kohm, 5%, 1005	ROHM	2007-000153	
R154	R-Chip, 22Kohm, 5%, 1005	ROHM	2007-000153	
R155	R-Chip, 10Kohm, 5%, 1005	ROHM	2007-000148	
R156	R-Chip, 270ohm, 5%, 1005	ROHM	2007-001311	
R157	R-Chip, 270ohm, 5%, 1005	ROHM	2007-001311	
R158	R-Chip, 4.7Kohm, 5%, 1005	ROHM	2007-000143	
R159	R-Chip, 470ohm, 5%, 1005	ROHM	2007-000932	
R161	R-Chip, 100ohm, 5%, 1005	ROHM	2007-000138	

NO	DESCRIPTION		SEC. CODE	REMARK
R162	R-Chip, 1Mohm, 5%, 1005	ROHM	2007-000170	
R163	R-Chip, 10Kohm, 5%, 1005	ROHM	2007-000148	
R164	R-Chip, 10Kohm, 5%, 1005	ROHM	2007-000148	
R165	R-Chip, 100ohm, 5%, 1005	ROHM	2007-000138	
R166	R-Chip, 100ohm, 5%, 1005	ROHM	2007-000138	
R301	NC	OPEN		
R302	R-Chip, 0ohm, 5%, 1005	ROHM	2007-000171	
R303	R-Chip, 10Kohm, 5%, 1005	ROHM	2007-000148	
R304	R-Chip, 10Kohm, 5%, 1005	ROHM	2007-000148	
R305	R-Chip, 91ohm, 5%, 2012	ROHM	2007-001247	
R306	R-Chip, 36ohm, 5%, 1005	ROHM	2007-001294	
R307	R-Chip, 36ohm, 5%, 1005	ROHM	2007-001294	
R308	R-Chip, 36ohm, 5%, 1005	ROHM	2007-001294	
R309	R-Chip, 3.3Kohm, 5%, 1005	ROHM	2007-001325	
R311	R-Chip, 1Kohm, 5%, 1005	ROHM	2007-000140	
R312	R-Chip, 22Kohm, 5%, 1005	ROHM	2007-000153	
R313	NC	OPEN		
R314	R-Chip, 100Kohm, 5%, 1005	ROHM	2007-000162	
R315	R-Chip, 3.9Kohm, 5%, 1005	ROHM	2007-007001	
R316	R-Chip, 56Kohm, 5%, 1005	ROHM	2007-000159	
R317	NC	OPEN		
R318	R-Chip, 100Kohm, 5%, 1005	ROHM	2007-000162	
R319	R-Chip, 2.2Kohm, 5%, 1005	ROHM	2007-000141	
R321	R-Chip, 33Kohm, 5%, 1005	ROHM	2007-000775	
R322	R-Chip, 10Kohm, 5%, 1005	ROHM	2007-000148	
R323	R-Chip, 10Kohm, 5%, 1005	ROHM	2007-000148	
R324	R-Chip, 10Kohm, 5%, 1005	ROHM	2007-000148	

NO	DESCRIPTION		SEC. CODE	REMARK
R325	R-Chip, 10Kohm, 5%, 1005	ROHM	2007-000148	
R326	R-Chip, 10Kohm, 5%, 1005	ROHM	2007-000148	
R327	R-Chip, 10Kohm, 5%, 1005	ROHM	2007-000148	
R328	R-Chip, 10Kohm, 5%, 1005	ROHM	2007-000148	
R329	R-Chip, 10Kohm, 5%, 1005	ROHM	2007-000148	
R331	R-Chip, 5.1Kohm, 5%, 1005	ROHM	2007-000144	
R333	R-Chip, 1.2Kohm, 5%, 1005	ROHM	2007-001319	
R334	R-Chip, 100Kohm, 5%, 1005	ROHM	2007-000162	
R335	R-Chip, 680ohm, 5%, 1005	ROHM	2007-001119	
R336	R-Chip, 10Kohm, 5%, 1005	ROHM	2007-000148	
R337	NC	OPEN		
R338	NC	OPEN		
R501	R-Chip, 47Kohm, 5%, 1005	ROHM	2007-000157	
R502	R-Chip, 470ohm, 5%, 1005	ROHM	2007-000932	
R503	R-Chip, 3.3Kohm, 5%, 1005	ROHM	2007-001325	
R504	R-Chip, 0ohm, 5%, 1005	ROHM	2007-000171	
R505	R-Chip, 75ohm, 5%, 1005	ROHM	2007-007009	
R506	R-Chip, 68ohm, 5%, 1005	ROHM	2007-001301	
R507	R-Chip, 10Kohm, 5%, 1005	ROHM	2007-000148	
R508	R-Chip, 0ohm, 5%, 1005	ROHM	2007-000171	
R509	R-Chip, 56Kohm, 5%, 1005	ROHM	2007-000159	
R510	R-Chip, 680ohm, 5%, 1005	ROHM	2007-001119	
R511	R-Chip, 15ohm, 5%, 1005	ROHM	2007-002965	
R512	NC	OPEN		
R513	R-Chip, 4.7Kohm, 5%, 1005	ROHM	2007-000143	
R514	R-Chip, 240ohm, 5%, 1005	ROHM	2007-007141	
R515	R-Chip, 240ohm, 5%, 1005	ROHM	2007-007141	

NO	DESCRIPTION		SEC. CODE	REMARK
R516	R-Chip, 82ohm, 5%, 1005	ROHM	2007-001217	
R517	R-Chip, 100ohm, 5%, 1005	ROHM	2007-000138	
R518	R-Chip, 82ohm, 5%, 1005	ROHM	2007-001217	
R519	R-Chip, 300ohm, 5%, 1005	ROHM	2007-007008	
R520	R-Chip, 18ohm, 5%, 1005	ROHM	2007-001288	
R521	R-Chip, 300ohm, 5%, 1005	ROHM	2007-007008	
R522	R-Chip, 33ohm, 5%, 1005	ROHM	2007-001292	
R523	R-Chip, 10Kohm, 5%, 1005	ROHM	2007-000148	
R524	R-Chip, 16ohm, 5%, 1005	ROHM	2007-003006	
R525	R-Chip, 16ohm, 5%, 1005	ROHM	2007-003006	
R526	R-Chip, 16ohm, 5%, 1005	ROHM	2007-003006	
R527	R-Chip, 910ohm, 5%, 1005	ROHM	2007-001317	
R528	R-Chip, 0ohm, 5%, 1005	ROHM	2007-000171	
R529	R-Chip, 1Kohm, 5%, 1005	ROHM	2007-000140	
R531	R-Chip, 2.7Kohm, 5%, 1005	ROHM	2007-000142	
R532	R-Chip, 2Kohm, 5%, 1005	ROHM	2007-000137	
R533	R-Chip, 10ohm, 5%, 1005	ROHM	2007-000172	
R534	R-Chip, 10ohm, 5%, 1005	ROHM	2007-000172	
R535	NC	OPEN		
R536	R-Chip, 1.8Kohm, 5%, 1005	ROHM	2007-001320	
R537	R-Chip, 510ohm, 5%, 1005	ROHM	2007-002796	
R701	R-Chip, 0ohm, 5%, 1005	ROHM	2007-000171	
R702	R-Chip, 10ohm, 5%, 1005	ROHM	2007-000172	
R703	R-Chip, 39Kohm, 1%, 1005	ROHM	2007-007134	
R704	R-Chip, 3.9Kohm, 5%, 1005	ROHM	2007-007001	
R705	R-Chip, 10Kohm, 5%, 1005	ROHM	2007-000148	
R706	R-Chip, 10Kohm, 5%, 1005	ROHM	2007-000148	

NO	DESCRIPTION		SEC. CODE	REMARK
R325	R-Chip, 10Kohm, 5%, 1005	ROHM	2007-000148	
R326	R-Chip, 10Kohm, 5%, 1005	ROHM	2007-000148	
R707	NC	OPEN		
R708	NC	OPEN		
R709	R-Chip, 0ohm, 5%, 1005	ROHM	2007-000171	
R711	R-Chip, 0ohm, 5%, 1005	ROHM	2007-000171	
R712	R-Chip, 1.8Kohm, 5%, 1005	ROHM	2007-001320	
R713	R-Chip, 10Kohm, 5%, 1005	ROHM	2007-000148	
R714	R-Chip, 10Kohm, 5%, 1005	ROHM	2007-000148	
R715	R-Chip, 100ohm, 5%, 1005	ROHM	2007-000138	
R716	R-Chip, 15Kohm, 1%, 1005	ROHM	2007-007132	
R717	R-Chip, 12Kohm, 1%, 1005	ROHM	2007-007309	
R718	R-Chip, 6.8Kohm, 5%, 1005	ROHM	2007-000146	
R719	R-Chip, 8.2Kohm, 5%, 1005	ROHM	2007-000147	
R721	R-Chip, 1.2Kohm, 5%, 1005	ROHM	2007-001319	
R722	R-Chip, 8.2Kohm, 5%, 1005	ROHM	2007-000147	
R723	R-Chip, 470ohm, 5%, 1005	ROHM	2007-000932	
R724	R-Chip, 150ohm, 5%, 1005	ROHM	2007-001306	
R725	R-Chip, 39ohm, 5%, 1005	ROHM	2007-001295	
R726	R-Chip, 150ohm, 5%, 1005	ROHM	2007-001306	
R727	R-Chip, 5.6Kohm, 5%,1005	ROHM	2007-000982	
R728	R-Chip, 4.7Kohm, 5%, 1005	ROHM	2007-000143	
R729	R-Chip, 0ohm, 5%, 1005	ROHM	2007-000171	
R733	R-Chip, 47Kohm, 1%, 1005	ROHM	2007-007139	
R734	R-Chip, 0ohm, 5%, 1005	ROHM	2007-000171	
R735	R-Chip, 0ohm, 5%, 1005	ROHM	2007-000171	
R736	R-Chip, 100Kohm, 5%, 1005	ROHM	2007-000162	

NO	DESCRIPTION		SEC. CODE	REMARK
R738	R-Chip, 100Kohm, 5%, 1005	ROHM	2007-000162	
R739	NC	OPEN		
T701	RF Chip Transformer, 100mW	HITACHI	GH26-40003A	
	IC-			
TH101	THERMISTOR-NTC, 10Kohm	MURATA	1404-001040	
TH701	THERMISTOR-NTC, 10Kohm	MURATA	1404-001040	
U102	VOLTAG REGULATOR, TPS7333Q 8P	TAXAS	1203-001335	
U104	VOLTAGE REGULATOR, MIC2941ABT	MICREL	1203-000650	
U105	POSI, FIXED Reg, KA7806T, 3P, DIP	MOTOROLA	1203-000283	
U106	POSI, ADJUST REG, 5237, 3P	MITSUBISHI	1203-000422	
U109	Voltage Regulator, 11233, 6P	TOKO	1203-000384	
U112	EEPROM	ATMEL	1103-001062	
U113	ENCODER/DECODER, ST5092TQFPTR	SGS-THOMSON	1204-001375	
U114	DATA COMM /GEN, Q5270, 176P, 3.3V	QUALCOMM	1205-001196	
U301	FLASH Memory, 29LV800,512Kx16bit,48P	FUJITSU	1107-001033	
U302	IC-SRAM, 68FS2000, 256Kx8bit, 32P	SEC	1106-001115	
U303	IC-CMOS Logic, 7S04, Inverter,5P	TOSHIBA	0801-000885	
U304	DRIVER/RECEIVER IC, DS14C335MSA	NATIONAL	1006-001098	
U305	NC	OPEN		
U501	IC-Voltage Regulator, 5205, 5P	TOSHIBA	1203-001256	
U502	FET-GAAS, GN2011, 5V, -4V, 60mA	MICREL	0505-001062	
U503	IC-AGC AMP, 5500, 16P, DUAL, 45dB	MATSUSHITA	1201-001075	
U504	IC-CASCODE AMP, 0916, 4P, 2.7V	QUALCOMM	1201-001248	
U505	IC-SYNTHESIZER, LMX2332LTMX, 20P	MOTOROLA	1209-001114	
U506	IC-CASCODE AMP, 0916, 4P, 2.7V	MOTOROLA	1201-001248	
U701	IC-IF CIRCUIT, CXA3003R-T6, 80P	NATIONAL	1204-001113	
U702	IC-TTL, 4W53, MUX/DEMUX, 8P	SONY	0803-003010	

NO	DESCRIPTION		SEC. CODE	REMARK
R738	R-Chip, 100Kohm, 5%, 1005	ROHM	2007-000162	
R739	NC	OPEN		
U703	IC-AGC AMP, 5505, SOP, 16P, DUAL	TOSHIBA	1201-001076	
U704	IC-MIXER, uPC8109T, SOP, 6P, 59MIL	QUALCOMM	1205-001253	
U705	IC-PREAMP, 01037, SOP, 6P, 59MIL	NEC	1201-001175	
U707	IC HYB, SCH-100, RI21002, SOP, 4P	MATSUSHITA	GH13-10560A	
U708	FREQ-ISOLATOR, 836MHz, 15dB	ROCKWELL	4709-000129	
U709	IC-Voltage Regulator, 5205, 5P	HITACHI	1203-001256	
U711	IC-OP AMP, 7101, SOT-23, 5P	MICREL	1201-001006	
	MAIN PCB (SCW-F200(REVER 2.0)	SEM	GH41-10622A	
	15 PIN CABLE (90mm)	SUNGJI	GH39-40517A	
	15PIN CABLE (90mm)	SUNGJI	GH39-40517A	
	JACK-MODULAR, DEK616PCB4-F(ST)	DAE EUN	3722-000309	
	HOOK SWITCH, SPPY12087A	ALPS	3409-000109	
	D-SUB CONNECTOR, 9P	WOYOUNG	3701-000215	
	Angle DIP CONNECTOR, 53048-1510	MOLEX	3711-003936	
	HOOK BOARD PCB	SAEHAN	GH41-10623A	
ASSY	HAND SET , SCW-F200/F2000 PUBLIC	SUNGJI	GH96-01089A	
	LCD MODULE	ORION	GH07-20534A	
	KEYPAD LED	SEC	0601-001197	
	Angle DIP CONNECTOR, 53048-1510	MOLEX	3711-003936	
	KEYPAD PCB	SAEHAN	GH41-10624A	
	DIPOLE ANT , DF-10, 824~894MHz	ACE TECH	GH42-10517A	
	BATTERY, NI-MH, 4.8V, 1800mAh	DAE YUN	GH43-10105A	
	Adaptor, AC220V, 50Hz, DC11V, 800mA	DOO SUNG	GH44-30543A	

11. Function of Active Devices

Mobile Station Modem

1 Overview

1.1 Application Description

The dual-mode code-division multiple-access advanced mobile phone system (CDMA/AMPS) cellular telephone, is a complex consumer communications instrument that relies heavily upon digital signal processing. To simplify the design and reduce the production cost of a subscriber unit, QUALCOMM has developed a Mobile Station Modem (MSM2300), an Analog Baseband Processor (BBA2), and Automatic Gain Control (AGC) Amplifiers, Q5500 and Q5505. These devices perform all of the signal processing in the subscriber unit, from intermediate frequency (IF) to audio.

The QUALCOMM MSM2300 is a 4th-generation device. The MSM2300 integrates functions that support a dual-mode CDMA/FM subscriber unit. Subsystems within the MSM2300 include a CDMA processor, a Digital FM (DFM) processor, a QUALCOMM Code Excited Linear Predication (QCELP) Vocoder, a 80C186EC microprocessor, and assorted peripheral interfaces that are used to support other functions. Through integration and advanced functionality, the MSM2300 consumes less power and provides more flexibility than QUALCOMM's MSM2.2.

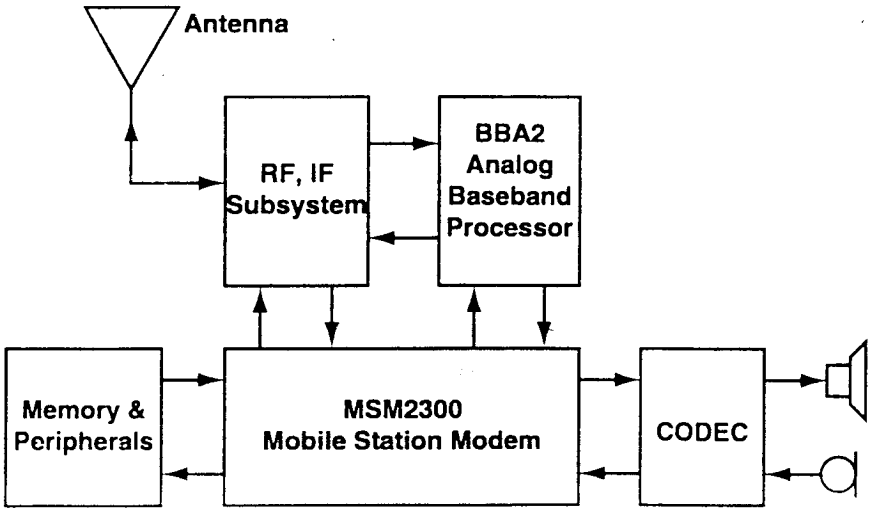


Figure 1-1 Typical Subscriber Unit Block Diagram

The MSM2300 (Figure 1-1) demodulates Rx digital baseband data from the BBA2. The BBA2 converts the modulated IF signal from the RF section of the subscriber unit into digital baseband data. For transmission, the MSM2300 modulates and sends digital baseband data to the BBA2. The Tx signal path of the BBA2 converts Tx digital baseband data into modulated IF. The MSM2300 communicates with the external RF and analog

baseband circuitry of the subscriber unit to control signal gain in the RF Rx a signal paths, null baseband offset errors and tune the system frequency refe

The MSM2300 performs baseband digital signal processing and executes the subscriber unit system software. It is the central interface device in the subscribe correlating RF, baseband and audio circuits, as well as memory and user interf features. The user interface of the subscriber unit typically includes the keypad, display, ringer, microphone and earpiece. These are either under the direct or in control of the MSM2300. The MSM2300 also contains complete digital modu and demodulation systems for both CDMA and AMPS cellular standards, as sp in IS-95-A.

The subscriber unit system software controls most of the functionality and acti the features of the subscriber unit. System software is executed by an embedde 80C186EC microprocessor within the MSM2300.

The CODEC interfaces directly with the microphone and earpiece, converting a audio signals from the microphone into digital signals for the Vocoder. The CC also converts digital audio data from the Vocoder into analog audio for the ear The MSM2300 supports an auxiliary external Pulse Coded Modulation (PCM interface. The auxiliary CODEC is optional within the subscriber unit.

The MSM2300 is available in three package styles. A 208-pin Plastic Quad Flat (PQFP) is available for low-volume system development applications. The 208 version allows connection to an MSM In-Circuit Emulator (MICE) for softwa development purposes. For high-volume subscriber unit production, a 176-pin Quad Flat Pack (TQFP) package is available. This package style does not allow to the MICE mode. A Pin-Bali Grid Array (PBGA) package is also available. F package dimensions, refer to Chapter 6 of this manual.

The MSM2300 is fabricated in an advanced submicron CMOS process. The d operates between 2.7 and 3.6 V for low-power consumption and long talk time the subscriber changes modes, the MSM2300 powers down unused circuits to power consumption to a minimum.

The MSM2300's electrical specifications, mechanical specifications and pin fun are compatible with the MSM2.2. The MSM2300 has many internal function enhancements and new debugging features, yet the programming requirements remained as backwardly compatible as possible allowing a smooth migration fro MSM2.2.

1.2 MSM2300 Features

MSM2300 General Features

- Supports IS-95-A compliant CDMA and AMPS subscriber units
- Low 2.7 to 3.6 Vdc power consumption during operation
- Internal DFM subsystem for AMPS operation (with BBA2)
- Software-controlled power management features
- Advanced submicron CMOS design
- Three package versions available. A 176-pin version for high-volume production and a 208-pin development version. (The 208-pin version supports MICE for System Development). A PBGA package is also available.
- ANSI/IEEE 1149.1 Testability

MSM2300 Audio Processing Features

- Internal 8 kbps Vocoder
- Internal 13 kbps Vocoder
- Support for 9600 bps and 14.4 kbps data rates
- Support for an external, user-supplied Vocoder
- Internal dual-tone multiple-frequency (DTMF) generation.
- Internal DTMF detection (CDMA mode only)
- Internal Earseal Echo Cancellation (ESEC) (CDMA mode only)
- Programmable digital filters for audio signal path compensation in both CDMA and AMPS modes
- Supervisory Audio Tone (SAT) transponding in FM mode
- Internal Voice Operated Switch (VOX)

Microprocessor Subsystem

- Embedded industry standard Intel 80C186EC microprocessor subsystem
- Internal watchdog and sleep timers
- Internal interrupt controller with support for both internal and off-chip interrupt driven devices
- Internal DMA controller with support for searcher DMA transfers (on-chip only)
- Internal chip select circuitry with direct support for RAM, ROM/FLASH, EEPROM, an LCD, and two other devices
- Microprocessor powerdown mode
- Internal address latches for demultiplexed address/data busses
- Internal programmable wait state generator
- Designed to operate with up to 20 MHz microprocessor clock rates

MSM2300 Supported Interface Features

- Support for handset and carkit CODECS in μ-Law, A-Law, or linear mode from various manufacturers
- Internal asynchronous serial data port with 64 byte Rx and 64 byte Tx FIFO buffers with hardware flow control
- Direct interface to Baseband Analog Processor (BBA2/Q5312)
- More than 30 general purpose I/O pins (several with interrupt capability)
- Support for an external keypad
- Support for up to 1 MByte of external RAM & ROM, and supports up to 1 MByte of EEPROM with optional bank switching
- Support for either 8-bit or 16-bit external RAM
- Three spare Pulse Density Modulated (PDM) outputs for user-defined analog control
- One spare general purpose programmable M/N counter output
- One programmable ringer output

- Internal ringer generation circuitry (without driver)

MSM2300 Enhancements over MSM2.2

- Through new architecture and circuit design, the MSM2300 consumes significantly less power and provides more flexibility than QUALCOMM MSM2.2
- The MSM2300 searcher engine can operate at rates up to eight times faste the searcher provided in the MSM2.2, allowing for faster acquisition and ne list search intervals. The MSM2300 searcher reports the best four local ma peaks per search window, reducing microprocessor overhead. Also, the MSM searcher reports the position of the multipath peaks with a higher resolutio allowing greater precision than the searcher provided in the MSM2.2.
- The MSM2300 uses an enhanced Viterbi decoder; which in some situatio results in a 0.5 - 0.7 dB improvement in 14.4 kbps rateset operation as com with the MSM2.2.
- The MSM2300's RF subsystem has been enhanced over the MSM2.2 to im intermodulation spurious response attenuation as outlined in IS-98, section
- The MSM2300 Vocoder clock source is more flexible than the MSM2.2, an includes XTAL_IN DIV 3, GPIO28 DIV 2, XTAL_IN DIV 2, CHIPX8 GPIO28 each as possible clock sources.
- The UART's Rx and Tx FIFO sizes are double the FIFO sizes of the MSM
- The MSM2300's internal 80C186EC serial port is available for use as a sec UART.
- The MSM2300 M/N counter has a larger range than the M/N counter pro in the MSM2.2.
- The MSM2300 has improved clock management features over the MSM2.
- Microprocessor powerdown during Slotted Paging Mode is now supported.
- The MSM2300's electrical specifications, mechanical specifications and pin functions are compatible with the MSM2.2. The MSM2300 has many inte functional enhancements and new debugging features, yet the programmin requirements have remained as backwardly compatible as possible, allowing smooth migration from the MSM2.2.
- The MSM2300 includes a fourth demodulating finger that increases the performance of the demodulator.

3.4 176 Pin Des[illegible] (Sorted by Pin Number)

[illegible] and Table 3.2 show the pin numbers and pin names for the 176 pin package MSM2300. Table 3.2, which lists the pin names by number, also provides t pin descriptions, pin type and pin drive strengths. The listing is sorted in numeric order.

Because the 176 pin package is intended for use in a mobile unit, it does not conta the interface required to support external processor emulation, and therefore cannc operate with an external processor or emulator. The 176 pin package MSM2300 is available in a TQFP (Thin Quad Flat Pack) form factor.

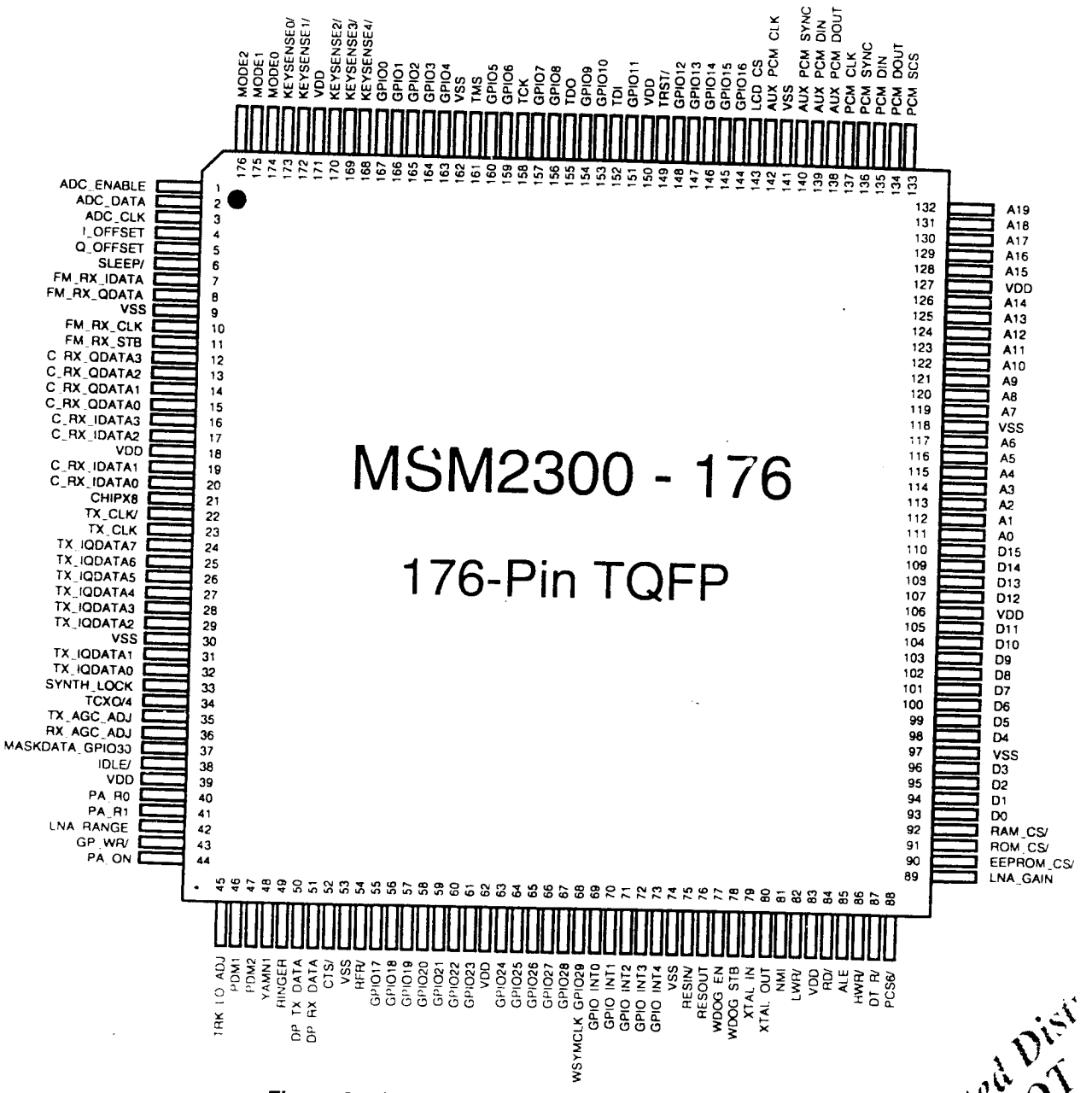


Figure 3-1 MSM2300–176 Pin Assignment Diagram

Table 3.2 176 Pin Description

176-Pin Number	Pin Name	Type	Pin Description	I_o [1] (mA)
1	ADC_ENABLE	ZH	When this output goes high, the General-Purpose ADC on BBA2 initiates an analog-to-digital conversion.	1.0
2	ADC_DATA	IXD	Serial data input from the General-Purpose ADC on BBA2.	pd
3	ADC_CLK	IHD	Clock input from the General-Purpose ADC on BBA2. When high, ADC_DATA is valid.	pd
4	I_OFFSET	ZPD	PDM output from the I-channel offset correction loop. I_OFFSET reduces offset errors on I-channel data.	2.0, pd
5	Q_OFFSET	ZPD	PDM output from the Q-channel offset correction loop. Q_OFFSET reduces offset errors on Q-channel data.	2.0, pd
6	SLEEP/	ZL	This output is low when the subscriber unit is in SLEEP mode. SLEEP/ can be used to disable unused circuits in the subscriber unit.	5.0
7	FM_RX_IDATA	IXD	Serial data input for 8-bit FM Rx I-channel data from BBA2.	pd
8	FM_RX_QDATA	IXD	Serial data input for 8-bit FM Rx Q-channel data from BBA2.	pd
9	V_{SS}	G	Ground	-
10	FM_RX_CLK	ZX	Clock output to the Rx FM ADCs on BBA2.	1.0
11	FM_RX_STB	ZH	Strobe output to the Rx FM ADCs on BBA2. When high, initiates the FM ADCs to do an analog-to-digital conversion.	1.0
12	C_RX_QDATA3	IXD	Q-channel data (C_RX_QDATA[3:0]) bits from the CDMA ADC on BBA2.	pd
13	C_RX_QDATA2	IXD		pd
14	C_RX_QDATA1	IXD		pd
15	C_RX_QDATA0	IXD		pd
16	C_RX_IDATA3	IXD	I-channel data (C_RX_IDATA[3:0]) bits from the CDMA ADC on BBA2.	pd
17	C_RX_IDATA2	IXD		pd
18	V_{DD}	V	Power Supply Voltage	-
19	C_RX_IDATA1	IXD	I-channel data (C_RX_IDATA[3:0]) bits from the CDMA ADC on BBA2.	pd
20	C_RX_IDATA0	IXD		pd
21	CHIPX8	IXD	9.8304 MHz clock input from BBA2. CHIPX8 is used primarily for CDMA hardware functions and vocoder processing.	pd
22	TX_CLK/	ZX	Clock output for the CDMA Q-channel transmit DAC. Clock input for FM transmit DAC.	2.0
23	TX_CLK	ZX	Clock output for the CDMA I-channel transmit DAC.	2.0

Table 3.2.1.5 Pin Description (continued)

176-Pin Number	Pin Name	Type	Pin Description	I_o [1] (mA)
24	TX_IQDATA7	ZX	I- and Q-channel Tx data (TX_IQDATA[7:0]) bits from MSM2300 to BBA2.	1.0
25	TX_IQDATA6	ZX		1.0
26	TX_IQDATA5	ZX		1.0
27	TX_IQDATA4	ZX		1.0
28	TX_IQDATA3	ZX		1.0
29	TX_IQDATA2	ZX		1.0
30	V_{SS}	G	Ground	-
31	TX_IQDATA1	ZX	I- and Q-channel Tx data (TX_IQDATA[7:0]) bits from MSM2300 to BBA2.	1.0
32	TX_IQDATA0	ZX		1.0
33	SYNTH_LOCK	IH	Indicates the lock status of UHF and IF frequency synthesizers. The SYNTH_LOCK input signal normally comes from the BBA2 and other frequency synthesizers in the subscriber unit's RF section.	In
34	TCXO/4	IXD	4.92 MHz clock input from BBA2.	pd
35	TX_AGC_ADJ	ZPD	PDM output from the Tx AGC subsystem. TX_AGC_ADJ controls Tx output power.	5.0, pd
36	RX_AGC_ADJ	ZPD	PDM output from the Rx AGC subsystem. RX_AGC_ADJ sets the Rx signal level in MSM2300.	5.0, pd
37	MASKDATA_GPIO30	BH	MASKDATA is active when the data of the current power control group is ready to transmit. If MASKDATA is not needed, this pin may be programmed to act as GPIO30. It is recommended that this pin be used as an output only.	5.0
38	IDLE/	BLD	Low when the subscriber unit is in IDLE mode. IDLE/ can be used to disable unused subscriber unit circuits. At RESOUT, IDLE/ is an input.	5.0 pd
39	V_{DD}	V	Power Supply Voltage	-
40	PA_R0	WP	Digital output from the CDMA Tx AGC loop. Can be used to alter RF power amplifier characteristics in the subscriber unit.	+2.0, od
41	PA_R1	WP		+2.0, od
42	LNA_RANGE	WP	Digital output from the CDMA Rx AGC loop. Can be used to alter low-noise amplifier characteristics or other stages in the subscriber unit's Rx signal path.	+2.0, od
43	GP_WR/	BL	Decoded general-purpose write strobe that can be used to control external general-purpose registers.	3.0,
44	PA_ON	ZH	This signal can control the RF power amplifier in the subscriber unit. PA_ON is high when the RF power amplifier is needed for a transmission.	5.0
45	TRK_LO_ADJ	ZP	PDM output from the frequency tracking subsystem in MSM2300. TRK_LO_ADJ sets the subscriber unit's IF and UHF frequencies.	5.0

Table 3.2 176 Pin Description (continued)

176-Pin Number	Pin Name	Type	Pin Description	I_O (mA)
46	PDM1	ZPD	General-purpose 8 bit PDM outputs clocked by TCXO/4 and under microprocessor control.	5.0, pd
47	PDM2	ZPD		5.0, pd
48	YAMN1	ZH	General-purpose microprocessor-programmable M/N counter that is clocked by TCXO/4.	1.0
49	RINGER	ZX	The signal on the RINGER output is from the MSM2300 DTMF tone generator. The DTMF generator selects the pitch and cadence of the subscriber unit 's ring. RINGER drives the sound transducer.	5.0
50	DP_TX_DATA	ZX	UART output.	3.0
51	DP_RX_DATA	IXD	UART input.	pd
52	CTS/	ILD	UART Clear-To-Send input signal.	pd
53	V_{SS}	G	Ground	-
54	RFR/	ZL	UART Ready-For-Receive output signal.	3.0
55	GPIO17	BXD	General-purpose I/O pin.In Vocoder Bypass mode this pin is VC_WR/, the external vocoder write strobe output.	1.0, pd
56	GPIO18	BXD	General-purpose I/O pin. In Vocoder Bypass mode this pin is VOC_FR_REF, the external vocoder frame-reference strobe output.	1.0, pd
57	GPIO19	BXD	General-purpose I/O pins which are programmed as inputs on RESOUT.	1.0, pd
58	GPIO20	BXD		1.0, pd
59	GPIO21	BXD		1.0, pd
60	GPIO22	BXD		1.0, pd
61	GPIO23	BXD		1.0, pd
62	VDD	V	Power Supply Voltage	-
63	GPIO24	BXD	General-purpose I/O pins which are programmed as inputs on RESOUT. GPIO28 may function as an external vocoder clock input in the MSM2300.	1.0, pd
64	GPIO25	BXD		1.0, pd
65	GPIO26	BXD		5.0, pd
66	GPIO27	BXD		5.0, pd
67	GPIO28	BXD		5.0, pd
68	WSYMCLK_GPIO29	BH	Outputs a pulse with a duration of one Walsh chip during the second Walsh symbol of every power control group. The placement of the pulse within the Walsh symbol is programmable. If the WSYMCLK feature is not needed, this pin may be programmed to function as GPIO29. It is recommended that this pin be used as an output only.	5.0

Table 3.2 176 Pin Description (continued)

176-Pin Number	Pin Name	Type	Pin Description	I_O [1] (mA)
69	GPIO_INT0	BPD	General-purpose I/O pins. The GPIO_INT[4:0] pins can cause an interrupt to the microprocessor. These pins are maskable, level-sensitive, and have programmable polarity.	1.0, pd
70	GPIO_INT1	BPD		1.0, pd
71	GPIO_INT2	BPD		1.0, pd
72	GPIO_INT3	BPD		1.0, pd
73	GPIO_INT4	BPD		1.0, pd
74	V_{SS}	G	Ground	-
75	RESIN/	BL	Hardware reset input to the '186 microprocessor.	3.0
76	RESOUT	BH	Reset output from the '186 microprocessor.	3.0
77	WDOG_EN	IHU	Watchdog Timer enable input.	pu
78	WDOG_STB	ZH	Watchdog Timer reset logic output.	1.0
79	XTAL_IN	IXA	Input connection point for an external quartz crystal or ceramic resonator. If an external oscillator is used, the output of the oscillator should be connected to this pin.	In
80	XTAL_OUT	ZXA	Feedback connection for an external quartz oscillator or ceramic resonator. If an external oscillator is used, this pin should be unconnected.	5.0
81	NMI	IHD	Non-maskable microprocessor interrupt input.	pd
82	LWR/	ZL	Low-byte write strobe from the CBIU.	3.0
83	VDD	V	Power Supply Voltage	-
84	RD/	BL	Read strobe output.	3.0
85	ALE	BH	Microprocessor address latch enable output.	3.0
86	HWR/	ZL	High-byte write strobe from the QBIU.	3.0
87	DT_R/	BX	Data transmit/receive control.	3.0
88	PCS6/	BL	Peripheral Chip Select 6. (output only)	3.0
89	LNA_GAIN	ZPD	PDM output from the RX AGC subsystem in the MSM2300. This signal, when filtered with a simple RC low-pass filter, is useful for controlling the gain of a variable gain low-noise amplifier (LNA).	5.0
90	EEPROM_CS/	ZL	QCSU EEPROM chip select.	3.0
91	ROM_CS/	ZL	QCSU ROM chip select.	3.0
92	RAM_CS/	ZL	QCSU RAM chip select.	3.0
93	D0	BXK	Data bus bits [3:0]	3.0
94	D1	BXK		3.0
95	D2	BXK		3.0
96	D3	BXK		3.0
97	V_{SS}	G	Ground	-

Table 3.2 176 Pin Description (continued)

176-Pin Number	Pin Name	Type	Pin Description	I_O [1] (mA)
98	D4	BXK	Data bus bits [11:4]	3.0
99	D5	BXK		3.0
100	D6	BXK		3.0
101	D7	BXK		3.0
102	D8	BXK		3.0
103	D9	BXK		3.0
104	D10	BXK		3.0
105	D11	BXK		3.0
106	V_{DD}	V	Power Supply Voltage	-
107	D12	BXK	Data bus bits [15:12].	3.0
108	D13	BXK		3.0
109	D14	BXK		3.0
110	D15	BXK		3.0
111	A0	ZX	Latched address bus bits [6:0].	3.0
112	A1	ZX		3.0
113	A2	ZX		3.0
114	A3	ZX		3.0
115	A4	ZX		3.0
116	A5	ZX		3.0
117	A6	ZX		3.0
118	V_{SS}	G	Ground	-
119	A7	ZX	Latched address bus bits [14:7].	3.0
120	A8	ZX		3.0
121	A9	ZX		3.0
122	A10	ZX		3.0
123	A11	ZX		3.0
124	A12	ZX		3.0
125	A13	ZX		3.0
126	A14	ZX		3.0
127	V_{DD}	V	Power Supply Voltage	-

Table 3.2 176 Pin Description (continued)

176-Pin Number	Pin Name	Type	Pin Description	I_O (mA)
128	A15	ZX	Latched address bus bits[19:15].	3.0
129	A16	BX		3.0
130	A17	BX		3.0
131	A18	BX		3.0
132	A19	BX		3.0
133	PCM_SCS	ZH	Serial PCM control select.	2.0
134	PCM_DOUT	ZXD	Serial PCM data output.	2.0, pd
135	PCM_DIN	IXD	Serial PCM data input	pd
136	PCM_SYNC	BHD	Data strobe for receive and transmit PCM data.	2.0, pd
137	PCM_CLK	BXD	Data clock for receive and transmit PCM data.	2.0, pd
138	AUX_PCM_DOUT	ZP	PCM data output for Auxiliary CODEC port.	3.0
139	AUX_PCM_DIN	IPU	PCM data input for Auxiliary CODEC port.	pu
140	AUX_PCM_SYNC	ZP	PCM data strobe for Auxiliary CODEC port.	3.0
141	V_{SS}	G	Ground	-
142	AUX_PCM_CLK	ZP	PCM data clock for Auxiliary CODEC port.	3.0
143	LCD_CS	ZH	Active high decoded chip select for LCD controller.	3.0
144	GPIO16	BXD	General-purpose I/O pin. In Vocoder Bypass mode this pin is VC_RD/, the external vocoder read strobe output.	1.0, pd
145	GPIO15	BXD	General-purpose I/O pin. In Vocoder Bypass mode this pin is VC_CS/, the external vocoder chip select output.	1.0, pd
146	GPIO14	BXD	General-purpose I/O pin. In Vocoder Bypass mode this pin is VC_ENC_INT, the external encoder interrupt input.	1.0, pd
147	GPIO13	BXD	General-purpose I/O pin. Programmed as an input on RESOUT. In Vocoder Bypass mode this pin is VC_DEC_INT, the external vocoder decoder interrupt input.	1.0, pd
148	GPIO12	BXD	General-purpose I/O pin, programmed as an input on RESOUT.	1.0, pd
149	TRST/	ILU	JTAG port reset input.	pu
150	V_{DD}	V	Power Supply Voltage	-
151	GPIO11	BXD	General-purpose I/O pin, programmed as an input on RESOUT.	1.0, pd
152	TDI	IXU	JTAG port data input.	pu
153	GPIO10	BXD	General-purpose I/O pins, programmed as inputs on RESOUT.	1.0, pd
154	GPIO9	BXD		1.0, pd
155	TDO	OX	JTAG port data output	

Table 3.2 176 Pin Description (continued)

176-Pin Number	Pin Name	Type	Pin Description	I (mA)
156	GPIO8	BXD	General-purpose I/O pins, programmed as inputs on RESOUT.	1.0, pd
157	GPIO7	BXU		1.0, pu
158	TCK	IXU	JTAG port clock input.	pu
159	GPIO6	BXU	General-purpose I/O pins, programmed as inputs on RESOUT.	1.0, pu
160	GPIO5	BXU		1.0, pu
161	TMS	IXU	JTAG port mode select input.	pu
162	V_{SS}	G	Ground.	-
163	GPIO4	BXU	General-purpose I/O pins, programmed as inputs on RESOUT.	1.0, pu
164	GPIO3	BXU		1.0, pu
165	GPIO2	BXU		1.0, pu
166	GPIO1	BXU		1.0, pu
167	GPIO0	BXU		1.0, pu
168	KEYSENSE4/	ILU	Can be used to sense key contact closure when connected to an external keypad. These pins require an active-low level-sensitive input signal. May cause an interrupt to the microprocessor.	pu
169	KEYSENSE3/	ILU		pu
170	KEYSENSE2/	ILU		pu
171	V_{DD}	V	Power Supply Voltage	-
172	KEYSENSE1/	ILU	Can be used to sense key contact closure when connected to an external keypad. These pins require an active-low level-sensitive input signal. May cause interrupt to the microprocessor.	pu
173	KEYSENSE0/	ILU		pu
174	MODE0	IXU	Selects the operating mode for the MSM2300: If MODE[2:0] = 111 NATIVE mode is selected If MODE[2:0] = 101 HI-Z mode is selected All other values for MODE[2:0] are reserved. DO NOT USE[2]. If unconnected, MODE[2:0] is pulled high selecting NATIVE mode. Vocoder Bypass (VOC_BYP) mode is selected by software only and is available under NATIVE mode.	pu
175	MODE1	IXU		pu
176	MODE2	IXU		pu

Notes for previous table:

1. Values 1.0, 2.0, 3.0, and 5.0 are the ± maximum current drive levels in mA for output pins. pd = internal pull-down resister on input pin, pu = internal pull up resister on input pin, od = open drain, In = no pull-up or pull-down resistor present when used as an input.
2. If any other modes are wired for prolonged periods, the device may be damaged. Mode[3:0] are internally pulled to 0b0111.

5.1 DC Electrical Specifications

5.1.1 Absolute Maximum Ratings

Operating the MSM2300 under conditions that exceed those listed in the Absolute Maximum Ratings Table may result in damage to the device. Absolute maximum ratings are limiting values, and are considered individually, while all other parameters are within their specified operating ranges. Functional operation of the MSM2300 under any of the conditions in the the Absolute Maximum Ratings Table is not implied.

Table 5.1 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units
T_S	Storage temperature	–65	+150	°C
T_J	Junction temperature		+150	°C
V_I	Voltage on any input or output pin	–0.5	V_{DD} + 0.5	V
V_{DD}	Supply voltage	–0.3	+4.6	V
I_{IN}	Latchup current		150	mA
V_{ESD}	Electrostatic discharge voltage (Human Body Model)		±2000	V

5.1.2 Recommended Operating Conditions

Table 5.2 Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units	Package
V_{DD}	Supply voltage	2.7	3.6	V	176
		3.3 -5%	3.3 +5%	V	208
T_A	Operating temperature	–40	85	°C	176
		0	70	°C	208

5.1.3 D.C. Characteristics

Table 5.3 D.C. Characteristics

Parameter		Min	Max	Units	Notes
V_{IH}	High–level input voltage, CMOS/Schmitt	0.65 V_{DD}	V_{DD} + 0.3	Volts	
V_{IL}	Low–level input voltage, CMOS/Schmitt	– 0.3	0.35 V_{DD}	Volts	
I_{IH}	Input high leakage current	-	2	µA	1
I_{IL}	Input low leakage current	-2	-	µA	1
I_{IHPD}	Input high leakage current with pull down	10	60	µA	1,2
I_{ILPU}	Input low leakage current with pull up	-60	-10	µA	2,3
I_{OZH}	High-level, three-state leakage current	-	2	µA	1
I_{OZL}	Low-level, three-state leakage current	-2	2-	µA	2
I_{OZHPD}	High-level, three-state leakage current with pull down	10	60	µA	1,3
I_{OZLPU}	Low-level, three-state leakage current with pull up	-60	-10	µA	2,3
I_{OZHKP}	High-level, three-state leakage current with keeper	-25	-3	µA	1,3
I_{OZLKP}	Low-level, three-state leakage current with keeper	3	25	µA	2,3
V_{OH}	High–level output voltage, CMOS/Schmitt	V_{DD} – 0.45	V_{DD}	Volts	4
V_{OL}	Low–level output voltage, CMOS/Schmitt	0.0	0.45	Volts	4
C_{IN}	Input capacitance		15	pF	

Notes for previous table:

1. Pin voltage = V_{DD} max. For keeper pins, pin voltage = V_{DD} max – 0.45 volts.
2. Pin voltage = Vss and V_{DD} = V_{DD} max. For keeper pins, pin voltage = 0.45 volts and V_{DD} = V_{DD} max.
3. Refer to table 3.1 in this manual for pins having pull ups, pull downs, and keepers
4. Refer to table 3.1 in this manual for I_{OH} and I_{OL} current capacity for output pins (at V_{DD} = V_{DD} min).

5.4 Power Consumption

These tables are an estimation of maximum operating currents for a nominal V_{DD}=3.3V. This information should be used as a general guideline for system design.

CDMA modes assume that the subscriber unit is operating in compliance with the CDMA specifications of IS–95–A. FM modes assume that the subscriber unit is operating in compliance with the AMPS specifications of IS–95–A. Estimates for maximum power supply current are under the following conditions: V_{DD}=3.3 Volts and T_A=25°C.

Table 5.4 Power Supply Currents for MSM2300 Operating Modes (Variable Rate Vocoding)

Symbol	Mode	Typical	Units
I_{DD1}	CDMA Rx/Tx (active full–duplex operation)[1]	65–85	mA
I_{DD2}	CDMA Rx (idle: CDMA Rx + processor + some "buffering" active; all else shut down)	40	mA
I_{DD3}	CDMA sleep (CDMA + processor in standby mode; some "buffering" active)	3	mA
I_{DD4}	FM Rx/Tx (active full–duplex operation)	35	mA
I_{DD5}	FM Rx (idle: receive channel active, transmit channel "off")	15	mA

Notes for previous table:

1. I_{DD1} is highly software dependent. It also depends upon vocoding rate, microprocessor clock frequency, and digital I/O load characteristics.

5.2 Timing Characteristics

5.2.1 CHIPX8 and TCXO/4 Timing

Figure 5-1 and Figure 5-2 show the timing characteristics between the two clocks (CHIPX8 and TCXO/4). The timing parameters are given in Table 5.5 and Table 5.6.

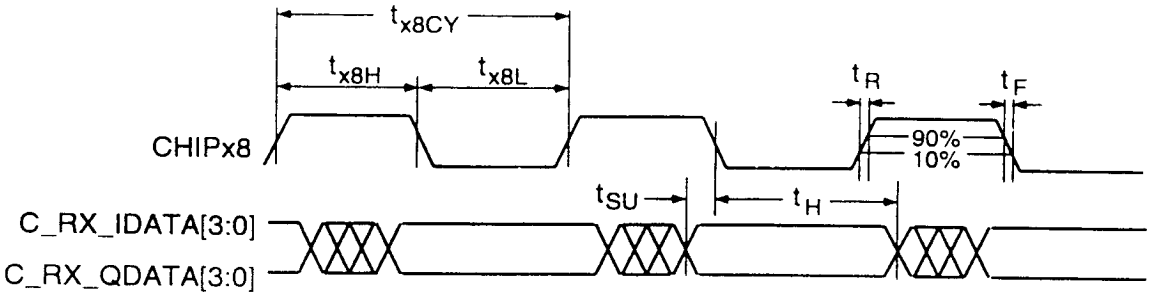


Figure 5-1 CDMA Rx Data Input Timing

Table 5.5 CDMA Rx Data Input Timing Parameters

Symbol	Parameter	Min	Type	Max	Units
t_{X8CY}	CHIPX8 period		101.7		ns
t_{X8H}	CHIPX8 logic high	40			ns
t_{X8L}	CHIPX8 logic low	40			ns
t_R	CHIPX8 risetime			12	ns
t_F	CHIPX8 falltime			12	ns
t_{SU}	Rx data input setup time	8			ns
t_H	Rx data input hold time	8			ns

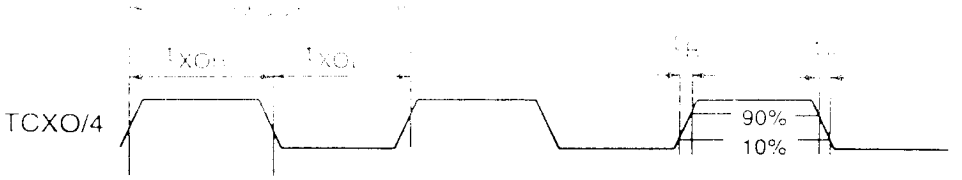


Figure 5-2 TCXO/4 Timing

Table 5.6 TCXO/4 Timing Parameters

Symbol	Parameter	Min	Type	Max	Units
t_{XOCY}	TCXO/4 period		203		ns
t_{XOH}	TCXO/4 logic high	75			ns
t_{XOL}	TCXO/4 logic low	75			ns
t_R	TCXO/4 risetime			12	ns
t_F	TCXO/4 falltime			12	ns

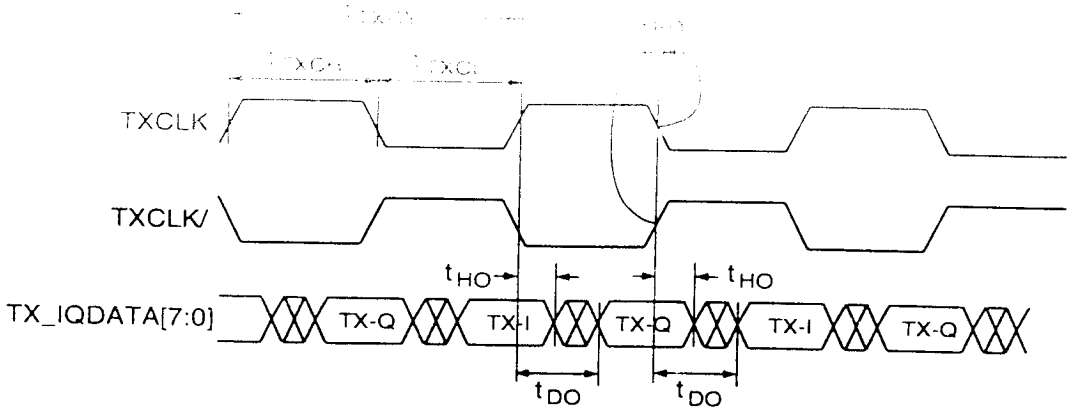


Figure 5-3 CDMA Tx Data Output Timing

Table 5.7 CDMA Tx Data Output Timing Parameters

Symbol	Parameter	Min	Type	Max	Units
t_{TXFCY}	TXCLK period		203		ns
t_{TXFCH}	TXCLK logic high		101		ns
t_{TXFCL}	TXCLK logic low		101		ns
t_{PD}	TXCLK to TCLK/ phase delay			1.2	ns
t_{DO}	Tx data output delay time			70	ns
t_{HO}	Tx data output hold time	20			ns

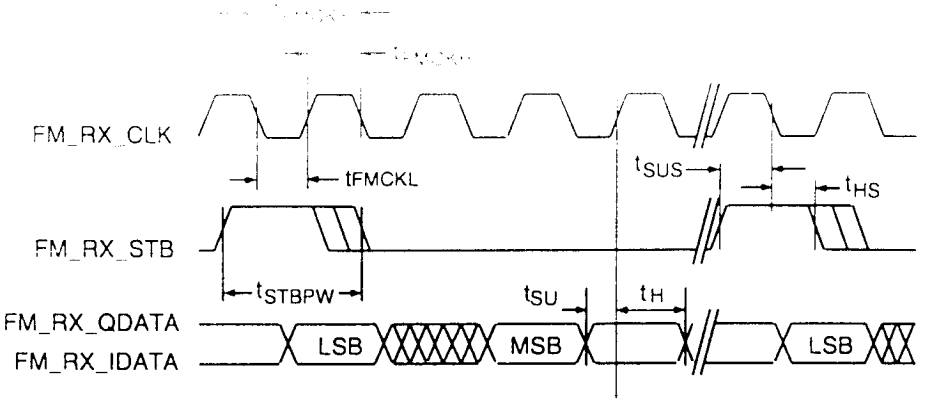


Figure 5-4 FM Rx Data Input Timing

Table 5.8 FM Rx Data Input Timing Parameters

Symbol	Parameter	Min	Type	Max	Units
t_{FMCKY}	FMCLK period		2.78		µs
t_{FMCKH}	FMCLK logic high		1.39		µs
t_{FMCKL}	FMCLK logic low		1.39		µs
t_{STBPW}	RXFMSTB pulse width		2.78		µs
t_{SUS}	RXFMSTB setup time	45			ns
t_{HS}	RXFMSTB hold time	10			ns
t_{SU}	RXQFMDATA, RXIFMDATA input setup time	10			ns
t_H	RXQFMDATA, RXiFMDATA input hold time	15			ns

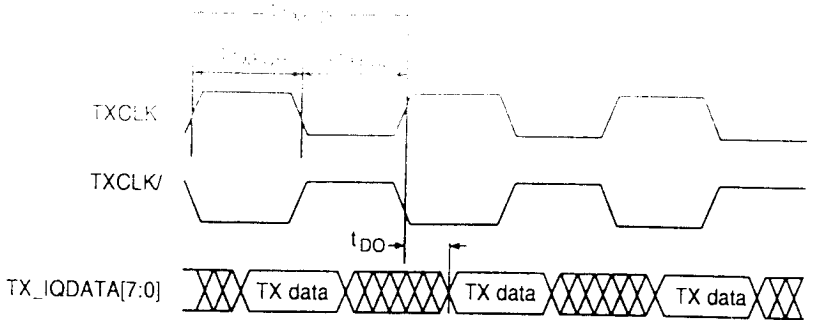


Figure 5-5 FM Tx Data Output

Table 5.9 FM Tx Data Output Timing Parameters

Symbol	Parameter	Min	Type	Max	Units
t_{TXFCY}	TXCLK period		8.33		µs
t_{TXFCH}	TXCLK logic high		4.17		µs
t_{TXFCL}	TXCLK logic low		4.17		µs
t_{DO}	Tx data output delay time			70	ns

General Purpose ADC Interface Timing

Figure 5-6 shows the ADC after it has first been initialized by a software reset. A software reset is followed by a start of conversion and then a read of converted data. ADC_RESET must occur prior to the first conversion request. This will drop ADC_ENABLE and prepare the ADC for the next data request. Software initiates a data transfer by writing to the ADC_DATA register. A start transfer request should be performed for each requested data value. Data is read once per conversion to avoid an overrun error. For additional information about the functionality of the registers in Figure 5-6, see page 4-140.

The parameters for the clock signal (t_{ckc}, t_{ckh}, and t_{ckl}) apply to every clock pulse for which there is a valid transfer of data.

Data is shifted from the BBA2, MSBit first. Each valid transfer consists of eight bits of data. The setup (t_s) and hold (t_h) times apply to each bit of ADC_DATA.

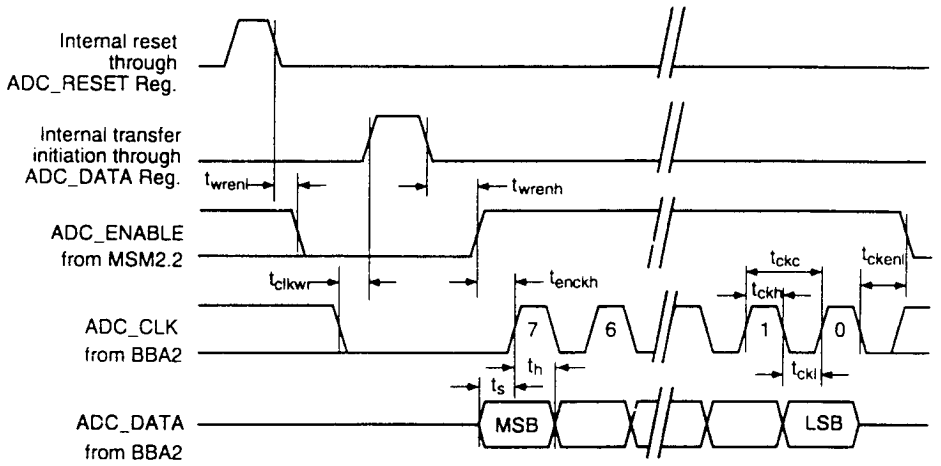


Figure 5-6 MSM2300 to ADC Timing Diagram

Table 5.10 MSM2300 to ADC Timing Parameters

Parameter	Description	Min	Typical	Max	Units
t_{cklwr}	ADC_CLK low before SW start of conversion write	0			ns
t_{wrenh}	Write of ADC_DATA register to ADC_ENABLE high			100	ns
t_{enckh}	ADC_ENABLE high to first ADC_CLK high	0.1	20		µs
t_{ckc}	ADC_CLK cycle time	0.100	2.4		µs
t_{ckh}	ADC_CLK pulse width high	0.025	1.2		µs
t_{ckl}	ADC_CLK pulse width low	0.025	1.2		µs
t_s	ADC_DATA setup time to positive edge ADC_CLK	20			ns
t_h	ADC_DATA hold time from positive edge ADC_CLK	20			ns
t_{ckeni}	Last ADC_CLK negative edge to ADC_ENABLE low			100	ns

[illegible] CODEC Timing

[illegible] timing values for Figure 5-7, Figure 5-8, and Figure 5-9.

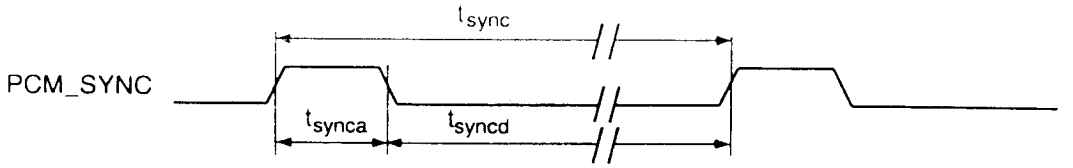


Figure 5-7 PCM_SYNC Timing

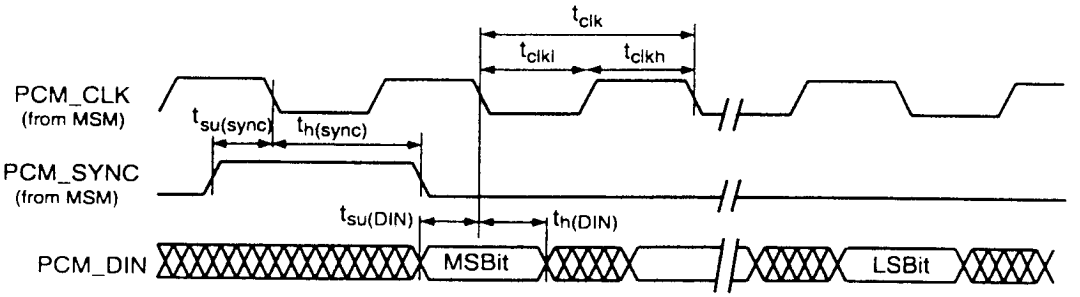


Figure 5-8 PCM_CODEC to MSM2300 Timing

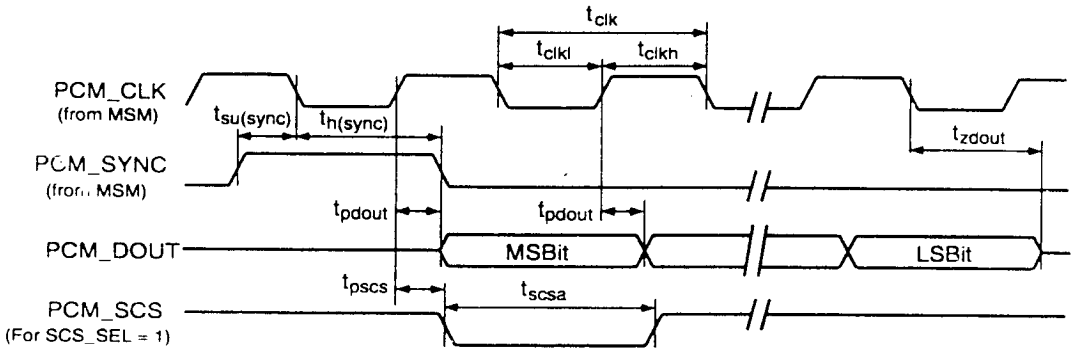


Figure 5-9 MSM2300 to PCM_CODEC Timing

Table 5.11 PCM_CODEC Timing Parameters

Parameter	Description	Min	Typical	Max	Units	Notes
t_{sync}	PCM_SYNC cycle time (PCM_SYNC_DIR=1)		125		µs	
	PCM_SYNC cycle time (PCM_SYNC_DIR=0)		125		µs	
t_{synca}	PCM_SYNC "asserted" time (PCM_SYNC_DIR=1)	400	500		ns	1
	PCM_SYNC "asserted" time (PCM_SYNC_DIR=0)				ns	
t_{syncd}	PCM_SYNC "deasserted" time (PCM_SYNC_DIR=1)		124.5		µs	1
	PCM_SYNC "deasserted" time (PCM_SYNC_DIR=0)				µs	
t_{clk}	PCM_CLK cycle time (PCM_CLK_DIR=1)	400	500		ns	1
	PCM_CLK cycle time (PCM_CLK_DIR=0)				ns	
t_{clkh}	PCM_CLK high time (PCM_CLK_DIR=1)	200	250		ns	1, 2
	PCM_CLK high time (PCM_CLK_DIR=0)				ns	
t_{clkl}	PCM_CLK low time (PCM_CLK_DIR=1)	200	250		ns	1, 2
	PCM_CLK low time (PCM_CLK_DIR=0)				ns	
$t_{su(sync)}$	PCM_SYNC setup time to PCM_CLK falling (PCM_SYNC_DIR = 1, PCM_CLK_DIR = 1)		150		ns	
	PCM_SYNC setup time to PCM_CLK falling (PCM_SYNC_DIR = 0, PCM_CLK_DIR = 0)				ns	
$t_{h(sync)}$	PCM_SYNC hold time after PCM_CLK falling (PCM_SYNC_DIR = 1, PCM_CLK_DIR = 1)		350		ns	
	PCM_SYNC hold time after PCM_CLK falling (PCM_SYNC_DIR = 0, PCM_CLK_DIR = 0)				ns	
$t_{su(din)}$	PCM_DIN setup time to PCM_CLK falling	75			ns	
$t_{h(din)}$	PCM_DIN hold time after PCM_CLK falling	30			ns	
t_{pdout}	Delay from PCM_CLK rising to PCM_DOUT valid			75	ns	
t_{zdout}	Delay from PCM_CLK falling to PCM_DOUT HIGH-Z		One Vocoder Clock Cycle			
t_{pcs}	Delay from PCM_CLK rising to PCM_SCS low			75	ns	3
t_{scsa}	PCM_SCS "asserted" time		500		ns	

Notes for previous table:

1. This value assumes that CODEC_CTL is not being used to override the CDMA CODEC clock and sync operation.
2. t_{clkh} and t_{clkl} are independent of PCM_CLK_SENSE.
3. This assumes that the AUX_CODEC_CONTROL:SCS_SEL is set (1). See Chapter 4 AUX_CODEC_CONTROL.

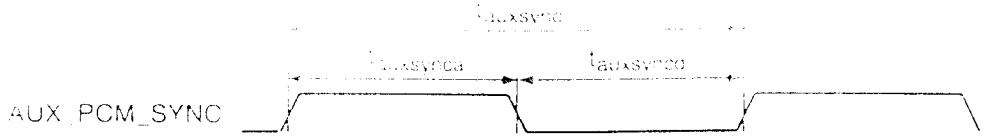


Figure 5-10 AUX_PCM_SYNC Timing

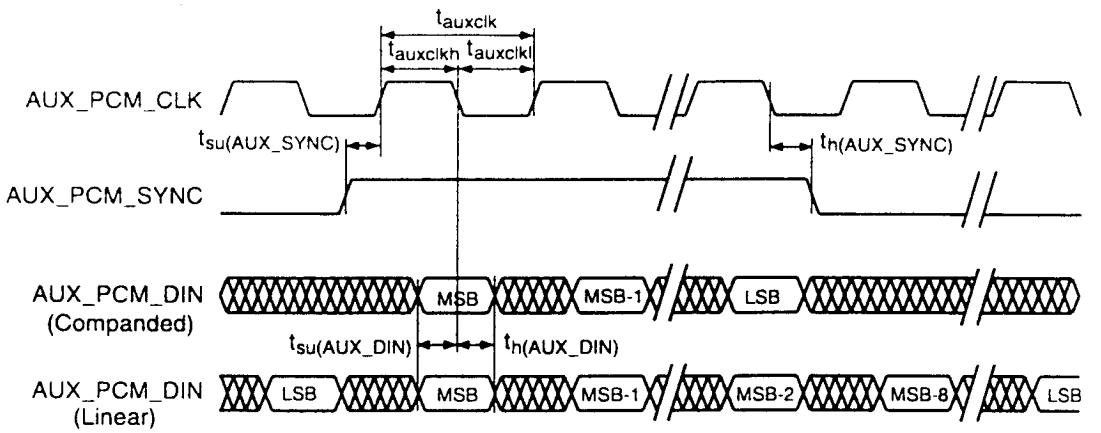


Figure 5-11 CODEC to MSM2300 Timing via AUX_CODEC (MSM2300 Receiving)

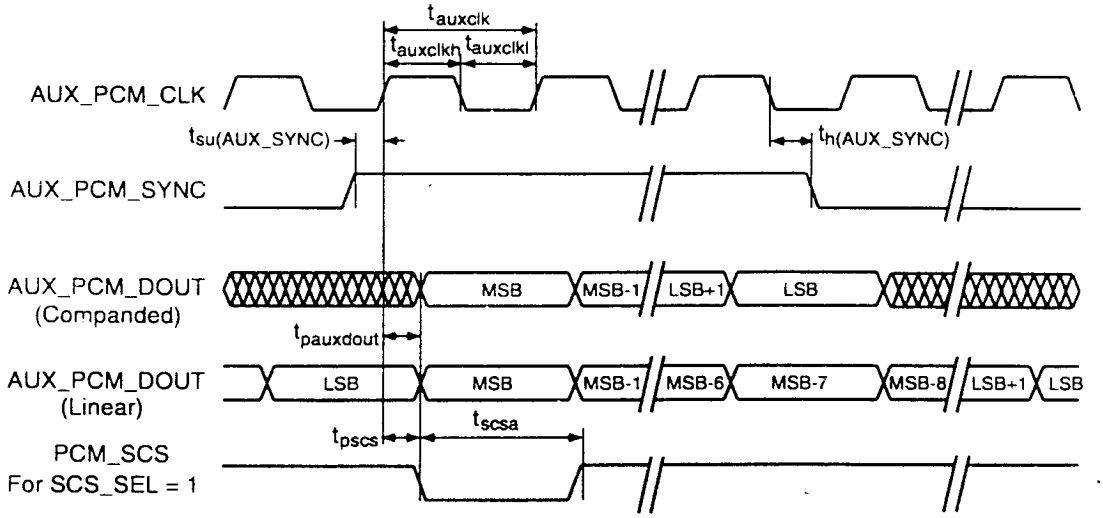


Figure 5-12 MSM2300 to CODEC Timing via AUX_CODEC (MSM2300 Transmitting).

Table 5.12 AUX CODEC Timing Parameters

Parameter	Description	Min	Typical	Max	Units	Notes
$t_{auxsync}$	AUX_PCM_SYNC cycle time		125		µs	
$t_{auxsynca}$	AUX_PCM_SYNC "asserted" time		62.5		µs	1
$t_{auxsyncd}$	AUX_PCM_SYNC "deasserted" time		62.5		µs	1
t_{auxclk}	AUX_PCM_CLK cycle time		7.8		µs	1
$t_{auxclkh}$	AUX_PCM_CLK high time	3.8	3.9		µs	1
$t_{auxclkl}$	AUX_PCM_CLK low time	3.8	3.9		µs	1
$t_{su(AUX\_SYNC)}$	AUX_PCM_SYNC setup time to AUX_PCM_CLK rising		1.95		µs	
$t_{h(AUX\_SYNC)}$	AUX_PCM_SYNC hold time after AUX_PCM_CLK rising		1.95		µs	
$t_{su(AUX\_DIN)}$	AUX_PCM_DIN setup time to AUX_PCM_CLK falling	75			ns	
$t_{h(AUX\_DIN)}$	AUX_PCM_DIN hold time after AUX_PCM_CLK falling	30			ns	
$t_{pauxdout}$	Propagation delay from AUX_PCM_CLK rising to AUX_PCM_DOUT valid			75	ns	
t_{pscs}	Propagation delay from AUX_PCM_CLK rising to PCM_SCS low.			75	ns	2
t_{scsa}	PCM_SCS "asserted" time		800		ns	2

Notes for previous table:

1. This value assumes that CODEC_CTL is not being used to override the CDMA CODEC clock and sync operation.
2. This assumes that the AUX_CODE_CONTROL:SCS_SEL is set (1). See Chapter 4 AUX_CODEC_CONTROL

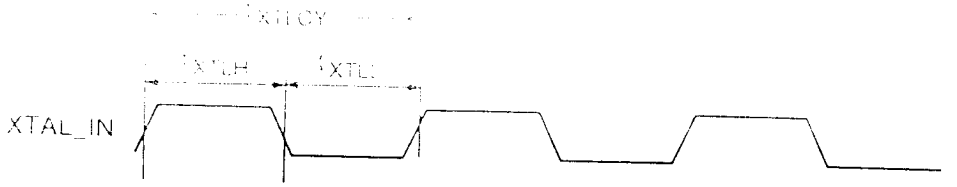


Figure 5-13 Crystal Timing Diagram

Table 5.13 Crystal Timing Requirements

Parameter	Description	Min	Type	Max	Units
t_{XTLKCY}	XTAL_IN period	25			ns
t_{XTLH}	XTAL_IN pulse width high	10			ns
t_{XTLL}	XTAL_IN pulse width low	10			ns

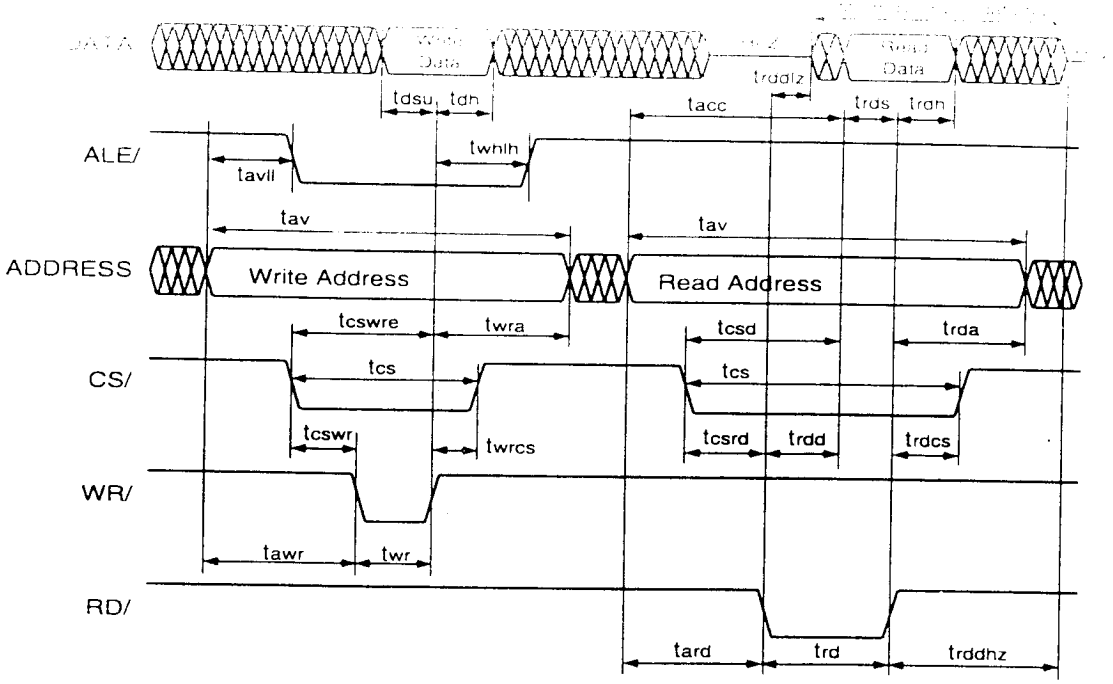


Figure 5-14 Microprocessor Bus Timing

Notes:
1. CS/ refers to RAM_CS/, ROM_CS/, and EEPROM_CS/.
2. WR/ refers to LWR/ and HWR/.

Table 5.14 Microprocessor Bus Timing Requirements

Parameter		Min	Max	Units	Notes
t_{av}	Address valid to address invalid	3.5T–50+nTW		ns	1
t_{cs}	Chip select active (pulse width)	3.5T–50+nTW		ns	2
t_{dsu}	Data setup prior to WR/ inactive	2T–70+nTW		ns	1, 2
t_{dh}	Data hold after WR/ inactive	T–30		ns	1, 2
t_{wra}	WR/ inactive to Address invalid	0.5T–15		ns	1, 2
t_{cswr}	Chip select active to WR/ active	T–40		ns	1, 2
t_{awr}	Address valid to WR/ active	T–40		ns	1, 2
t_{wr}	WR/ active (pulse width)	2T–30+nTW		ns	1, 2
t_{wrcs}	WR/ inactive to CS/ inactive	0.5T–15		ns	1, 2
t_{cswre}	CS/ active to WR/ inactive	3T–45+nTW		ns	1, 2
t_{csrd}	CS/ active to RD/ active	T–40		ns	1, 2

Table 5.2.4 Microprocessor Bus Timing Requirements (continued)

Parameter		Min	Max	Units	Notes
t_{rds}	Data setup to RD/ rising	40		ns	1, 2
t_{rdh}	RD/ rising to Data hold	0		ns	1, 2
t_{rda}	RD/ inactive to address invalid	0.5T–15		ns	1, 2
t_{ard}	Address valid to RD/ active	T–40		ns	1, 2
t_{rd}	RD/ active (pulse width)	2T–30+nTW		ns	1, 2
t_{acc}	Address valid to valid read data		3T–70+nTW	ns	1, 2
t_{rdd}	RD/ active to valid read data		2T–70+nTW	ns	3
t_{csd}	CS/ active to valid read data		3T–70+nTW	ns	3
t_{rdcs}	RD/ inactive to CS/ inactive	0.5 T–15		ns	3
t_{rddhz}	RD/ inactive to read data High-Z		T-15	ns	3
t_{rddlz}	RD/ active to read data low-Z	0		ns	3
t_{vall}	AD valid setup before ALE falls	.5T –10		ns	
t_{whlh}	WR rising to next ALE rising	.5T –10		ns	

Notes for previous table:

1. T, in the Min and Max columns, is the microprocessor clock cycle time and is a function of the cycle time at the XTAL_IN pin and the divider for the '186 microprocessor power save circuitry. T = (period of XTAL_IN/2) x (optional Power Save Mode).
2. "n_{TW}" is the integer number of wait–states multiplied by the µP clock cycle time (T).
3. Calculated value.

5.2.5 QBIU Parametrics

The QBIU takes each 16 bit RAM access and translates it into two sequential 8 bit RAM accesses. The QBIU works only with RAM_CS/.

Figure 5-15 shows a typical timing diagram for the QBIU operation. The upper ro shows the microprocessor's WAIT_STATES (identified as Tw1 through Tw7) that counts off the RAM_WORD+1 wait states. The second row, WR_CNT/RD_CNT counts off WR_CNT or RD_CNT Tcycles.

Figure 5-15 is not to scale and makes certain assumptions, such as:

1. A 16 bit RAM access is taking place to and from an 8 bit bus-sized RAM. Th 8 bit bus-sized RAM data connections are MSM2300 pins D[7:0].
2. RD/ is the read strobe.
3. Either LWR/ or HWR/ may be used as a write strobe for the RAM. Both signal provide write data strobing for a RAM.

5. RAM_WORD=6 generating a total of 7 Tw (wait Tcycles) for the entire operation. (RAM_WORD is programmed with one less than the total number of wait states for a RAM word access.)

6. WR_CNT=4 causing the end of the first byte operation after 4 wait Tcycles (Tw1, Tw2, Tw3, & TW4).

Table 5.15 quantifies the QBIU timing parameters for a typical bus sizer action.

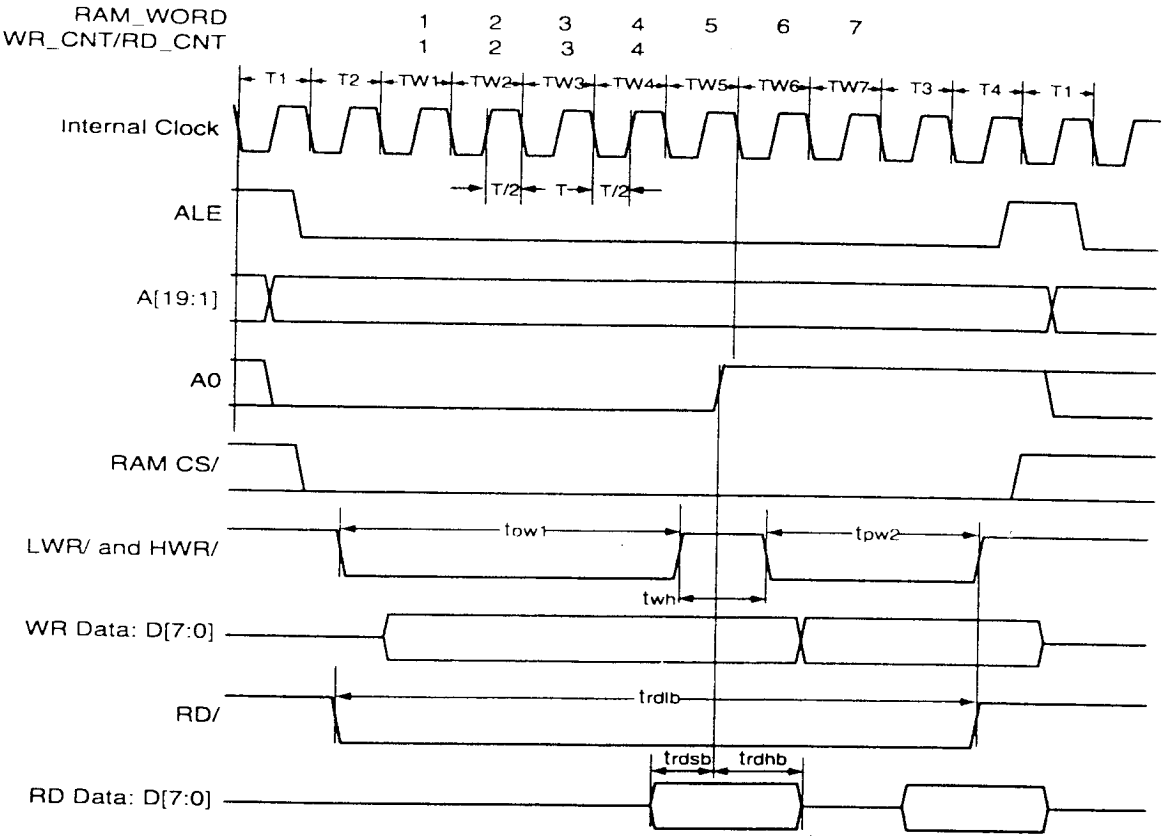


Figure 5-15 Bus Interface Unit Timing

Table 5.7.1 Bus Interface Unit Parameters in NATIVE Mode

Parameter	Description	Min	Typical	Max	Units	Notes
t_{pw1}	Pulse width of first LWR/ or HWR/ pulse		(X+1) ×T		ns	1,2
t_{wh}	Pulse width of LWR/ and HWR/ high in the middle of a cycle		T		ns	2
t_{pw2}	Pulse width of second LWR/ and HWR/ pulse		(Y–X) ×T		ns	1,2,3
t_{rdsb}	Required RD data setup in middle of bus sizer cycle	40			ns	4
t_{rdlb}	RD low time during bus sizer read		(Y+2) ×T		ns	3,2
t_{rdhb}	Required RD data hold in middle of bus sizer cycle	0			ns	4

Notes for previous table:

1. For a read cycle X=RD_CNT. For a write cycle X=WR_CNT. For proper bus sizer operation X>0.
2. T is the microprocessor clock cycle time. t= 2/f; where f is the frequency applied at XTAL_IN adjusted by the clock scaling, or power save mode. (Clock scaling can be ÷1, ÷4, ÷8, ÷16, ÷32, or ÷64)
3. Y=Total number of RAM word wait states (i.e. value of RAM_WORD + 1). For proper bus sizer operation Y>X+1.
4. t_{rds}, t_{rdh}, t_{rdsb}, t_{rdhb}, and t_{rdlb} only apply to read cycle data.

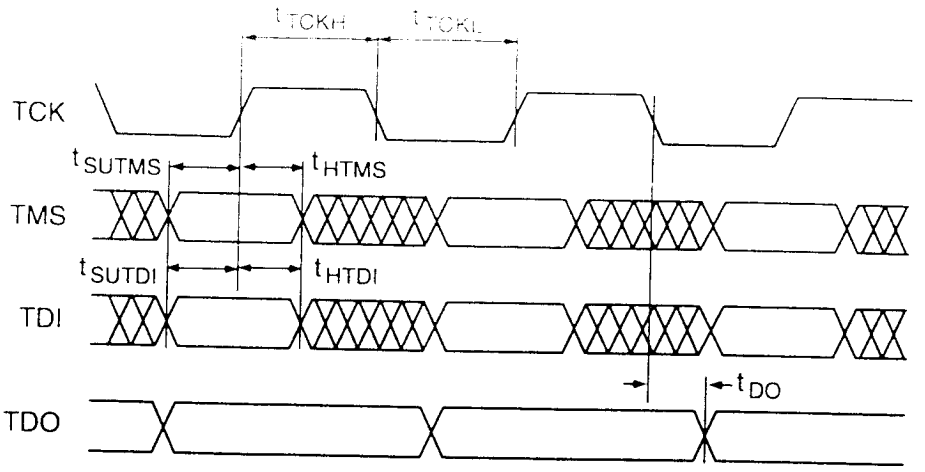


Figure 5-16 JTAG Interface Timing

Table 5.16 JTAG Interface Timing

Parameter	Description	Min	Typi-cal	Max	Units
t_{TCKCY}	TCK period)	500			ns
t_{TCKH}	TCK pulse width high	200			ns
t_{TCKL}	TCK pulse width low	200			ns
t_{SUTMS}	TMS Input Set-up Time	50			ns
t_{HTMS}	TMS Input Hold Time	50			ns
t_{SUTDI}	TDI Input Set-up Time	50			ns
t_{HTDI}	TDI Input Hold Time	50			ns
t_{DO}	TDO Data Output Delay			70	ns

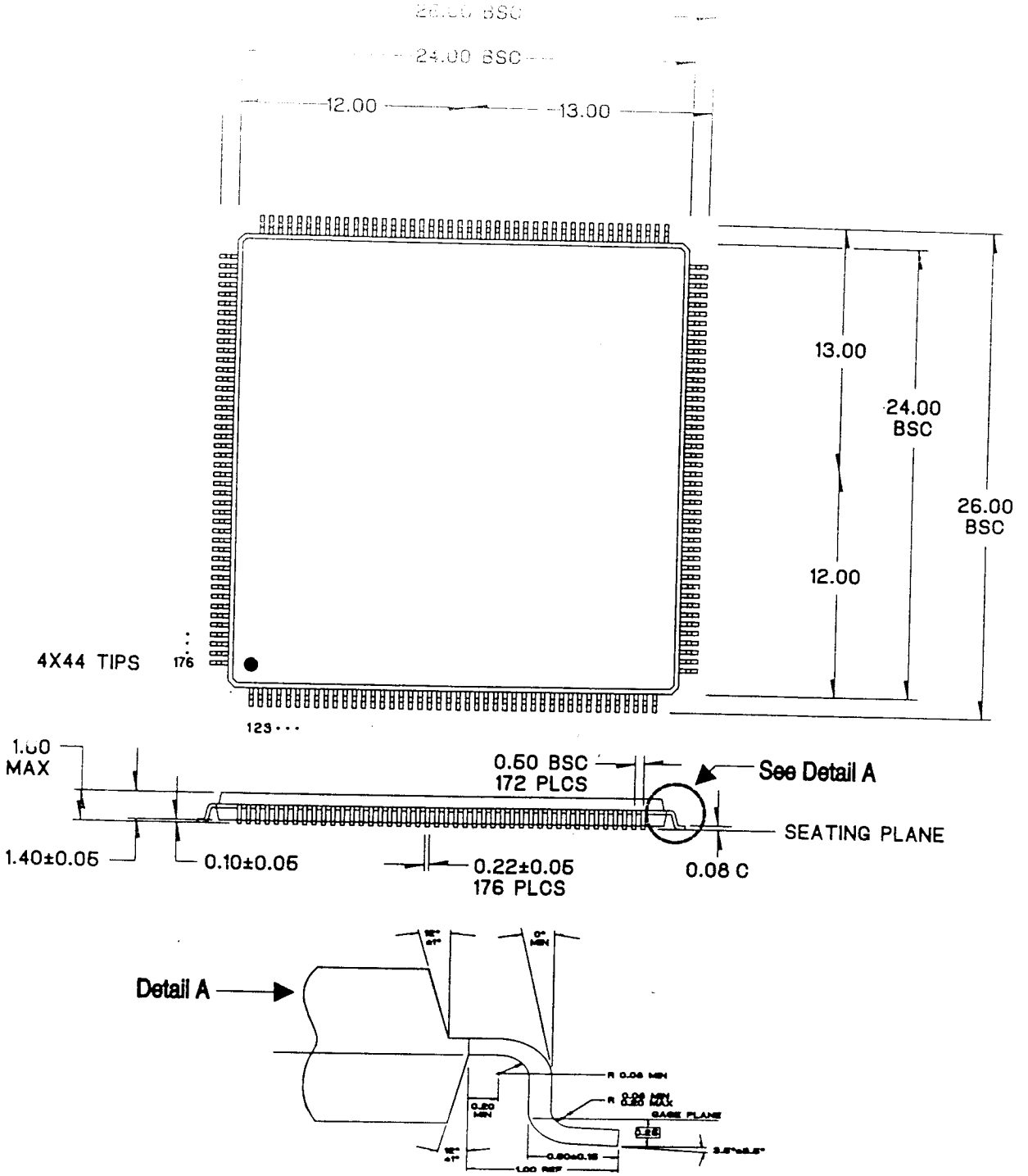


Figure 6-1 MSM2300 176 pin Package & Dimensions

Baseband Analog Procesor

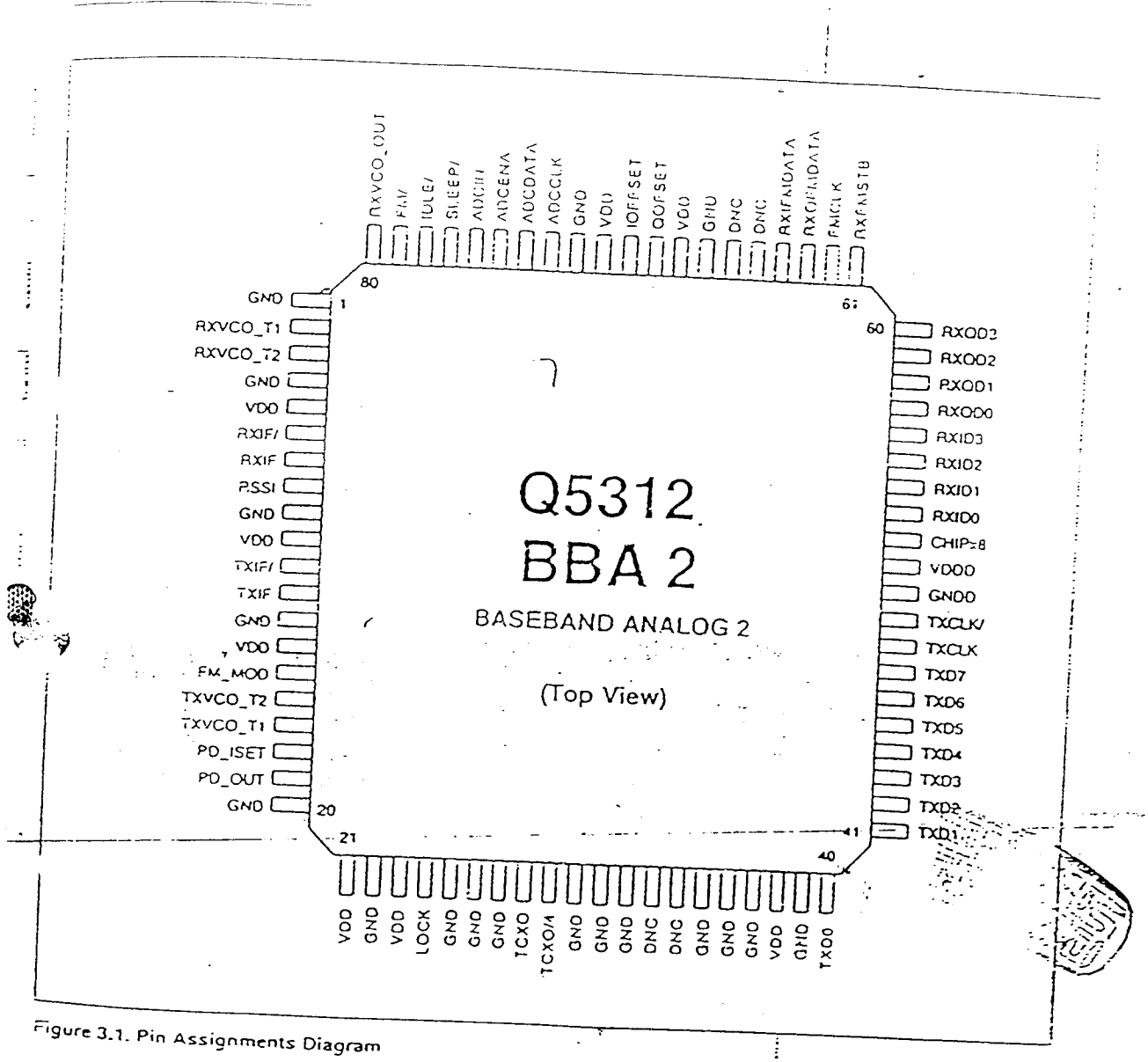


Figure 3.1. Pin Assignments Diagram

Table 3.1 Receive Signal Path Pins

Pin	Pin Name	I/O	Pin Description
			Receive Signal Path
2 3	RXVCO_T1 RXVCO_T2	AI	The receive VCO tuning points connect to an external LC tank circuit for precise setting of the receive VCO frequency. The receive VCO is active in RXTX and IDLE modes for CDMA and FM. In SLEEP mode, these pins are pulled high.
6, 7	RXIF/, RXIF	AI	Negative and positive analog differential receive IF inputs. These inputs are active in RXTX and IDLE modes for CDMA and FM. In SLEEP mode these pins are pulled low.
8	RSSI	AO	The analog RSSI detector output is active in CDMA RXTX and IDLE modes. When inactive, the output is pulled high.
53 54 55 56	RXID0 RXID1 RXID2 RXID3	DO	CDMA I receive data is output to the MSM 2 on this 4-bit port. RXID3 is the MSB. Active in CDMA RXTX and CDMA IDLE, otherwise logic low.
57 58 59 60	RXQD0 RXQD1 RXQD2 RXQD3	DO	CDMA Q receive data is output to the MSM 2 on this 4-bit port. RXQD3 is the MSB. Active in CDMA RXTX and CDMA IDLE, otherwise logic low.
61	RXFMSTB	DI	Receive FM data strobe. Active in FM RXTX and FM IDLE modes. Pulled low if left unconnected.
62	FMCLK	DI	Receive FM data clock. Active in FM RXTX and FM IDLE modes. Pulled low if left unconnected.
63	RXQFMDATA	DO	Receive FM Q serial data output. Active in FM RXTX and FM IDLE modes. Low when inactive.
64	RXIFMDATA	DO	Receive FM I serial data output. Active in FM RXTX and FM IDLE modes. Low when inactive.
69	QOFFSET	AI	Q Channel offset adjust input for CDMA and FM RXTX and IDLE modes. The MSM 2 derives a PDM signal which is filtered by an external RC at the pin.
70	IOFFSET	AI	I Channel offset adjust input for CDMA and FM RXTX and IDLE modes. The MSM 2 derives a PDM signal which is filtered by an external RC at the pin.
80	RXVCO_OUT	AO	Receive VCO output. Active in CDMA and FM RXTX and IDLE modes. Pulled low when inactive.

AI = analog input, AO = analog output, DI = digital input, DO = digital output

Table 3.2 Transmit Signal Path Pins

Pin	Pin Name	I/O	Pin Description
			Transmit Signal Path
11 12	TXIF/ TXIF	AO	Negative and positive analog differential transmit IF outputs. These pins are active in CDMA and FM RXTX modes. In all other modes, these pins are pulled high.
15	FM_MOD	AO	Analog FM modulation signal is active in FM RXTX mode only. When inactive, it is pulled low
16 17	TXVCO_T2 TXVCO_T1	AI	The transmit VCO tuning points connect to an external LC tank circuit for precise setting of the transmit VCO frequency. The transmit VCO is active in CDMA and FM RXTX modes. In all other modes, these pins are pulled to high.
40 41 42 43 44 45 46 47	TXD0 TXD1 TXD2 TXD3 TXD4 TXD5 TXD6 TXD7	DI	Transmit data input port from MSM 2. This port is active in CDMA and FM RXTX modes only. TXD7 is the MSB.
48 49	TXCLK TXCLK/	DI	Negative and positive differential transmit clock inputs. TXCLK and TXCLK/ are complementary inputs. These signals are 80° out of phase with respect to each other, ± 10% of rise/fall time. This clock is active in CDMA and FM RXTX modes only.

AI = analog input, AO = analog output, DI = digital input, DO = digital output

Table 3.3 Clock Synthesizer and Buffering Pins

Pin	Pin Name	I/O	Pin Description
			Clock Synthesis and Buffering
18	PD_ISET	AI	PD_OUT current set reference voltage. Active in CDMA and FM RX… modes. Pulled high if left unconnected.
19	PD_OUT	AO	Transmit synthesizer phase detector charge pump output… High-impedance when inactive.
24	LOCK	DO	Transmit IF synthesizer lock detect output. Active in CDMA and FM RX… modes. LOCK is an open drain, pulled high by an external pull-up resis… when inactive.
28	TCXO	DI	An externally generated 19.68 MHz clock frequency is applied to this pi… It is active in all modes.
29	TCXO/4	DO	A clock frequency equal to 1/4 of the TCXO frequency is output on this p… in all operating modes.
52	CHIPx8	DO	The CHIPx8 synthesizer is a digital divider with a ratio of 512/1025 time… the TCXO input frequency. As such, it will have an average output frequency of 9.8304 MHz, but will not have an exact 50% duty cycle. When the CHIPx8 synthesizer is disabled (CDMA SLEEP and FM EXT… Modes) the CHIPx8 signal is pulled to a logic low.

AI = analog input, AO = analog output, DI = digital input, DO = digital output

Table 3.4 General Purpose ADC and Mode Control Pins

Pin	Pin Name	I/O	Pin Description
			General Purpose ADC and Mode Controls
73	ADCCLK	DO	General Purpose ADC clock output. When high, valid data is available on ADCDATA. Low when inactive.
74	ADCDATA	DO	General Purpose ADC serial data output. Valid data is available here when ADCCLK is high. Low when inactive.
75	ADCENA	DI	The General Purpose ADC is enabled and a conversion is initiated by a positive-going pulse on this input. Pulled low when inactive.
76	ADCIN	AI	General Purpose A/D analog Input. The voltage applied to this input is digitized to 8-bit resolution by the General Purpose ADC when ADCENA is pulsed high.
77	SLEEP/	DI	CDMA SLEEP mode is invoked when this pin is low and FM/ is high. Pulled low if left unconnected.
78	IDLE/	DI	CDMA IDLE or FM IDLE modes are invoked when this input is low and SLEEP/ is high. Pulled low if left unconnected.
79	FM/	DI	FM or CDMA mode select. Pulled low if left unconnected.

AI = analog input, AO = analog output, DI = digital input, DO = digital output

Table 3.5 Power, Ground, and DNC Pins

Pin	Pin Name	I/O	Pin Description
Power, Ground, DNC			
5,10, 14, 21, 33, 58, 71	VDD	AI	+3.3 Volt Power Supply Input
51	VDDD	AI	+3.3 Volt Power Supply input for BBA 2 digital 4, 9
4, 9, 13, 20, 22, 37, 39, 67	GND	AI	Analog ground
50	GNDD	AI	Ground input for BBA 2 digital I/O
1, 25, 26, 27, 30, 31,32, 35, 36, 72	GND	AI	Analog grounds. These pins do not provide a current return path for BBA 2 but must be connected to GND.
33, 34, 65, 66	DNC		THESE PINS MUST BE LEFT UNCONNECTED

AI = analog input, AO = analog output, DI = digital input, DO = digital output

6 Packaging Information

The BBA 2 is packaged in an 80 Pin Thin Quad Flat Pack(TQFP). The TQFP has 20-mil lead pitch and no greater than 1.6 mm above the seating plane (JEDEC Publication 95 MO-136 Variation AM or BM.)

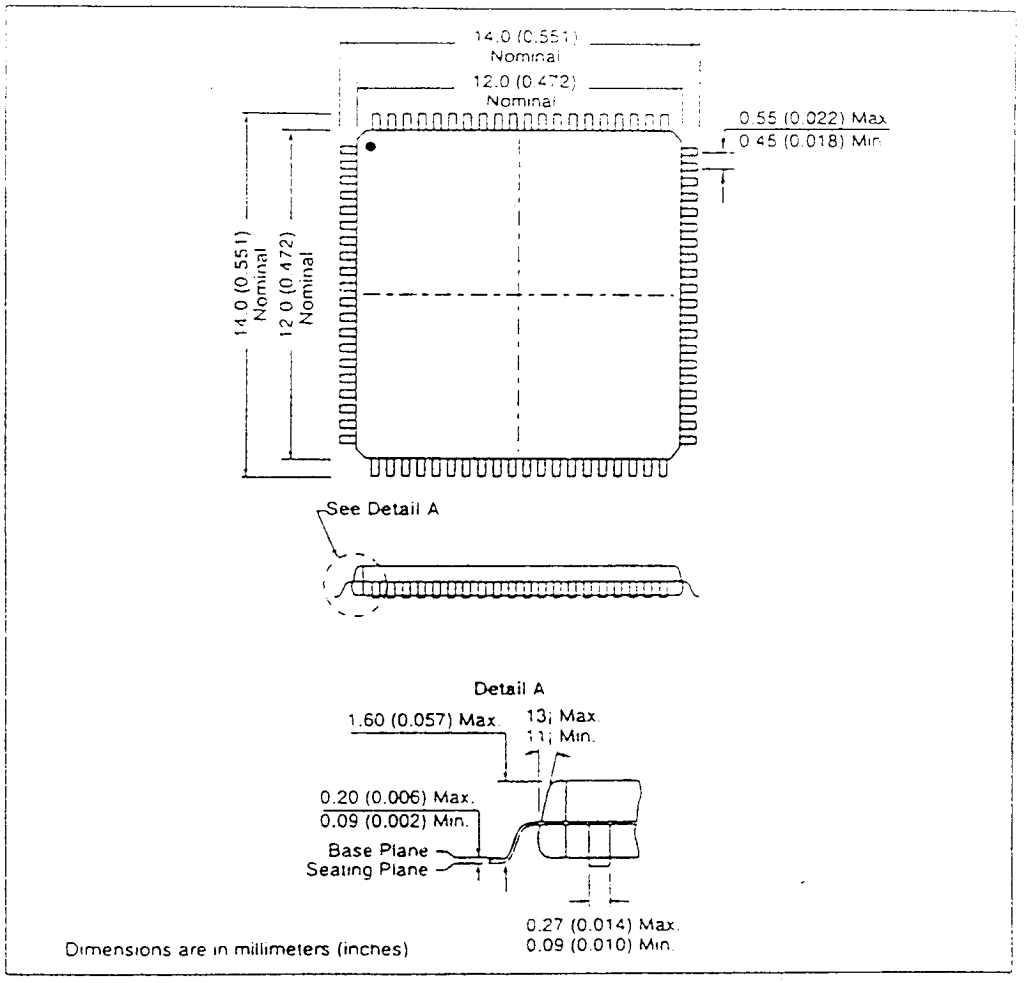


Figure 6.1. Detail Package Drawing

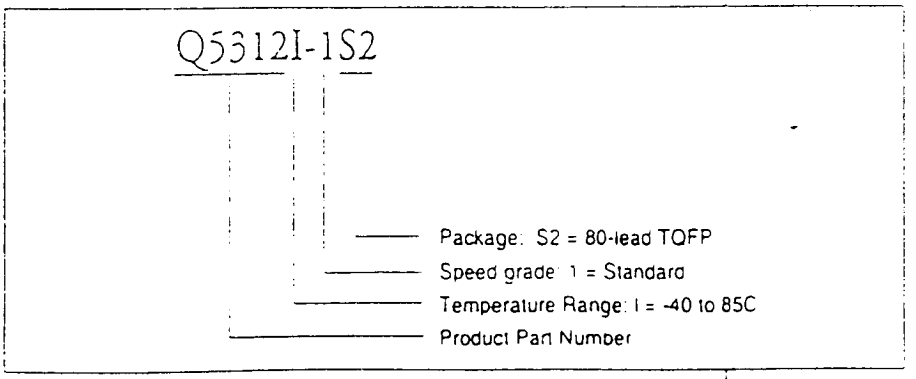
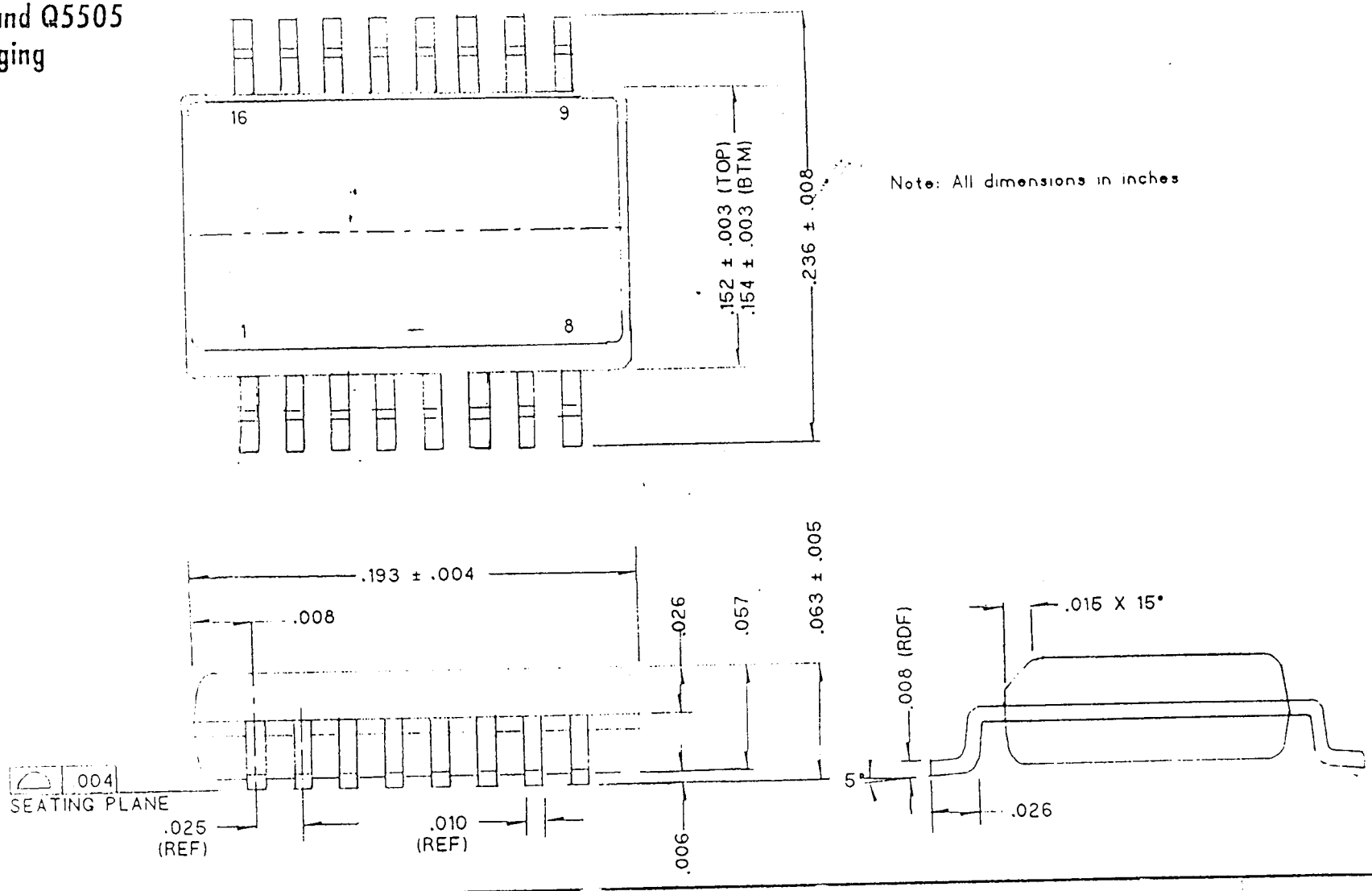


Figure 6.2. Package Markings

IF AGC Amplifier

Figure 16. Q5500 and Q5505
16-pin SSOP Packaging



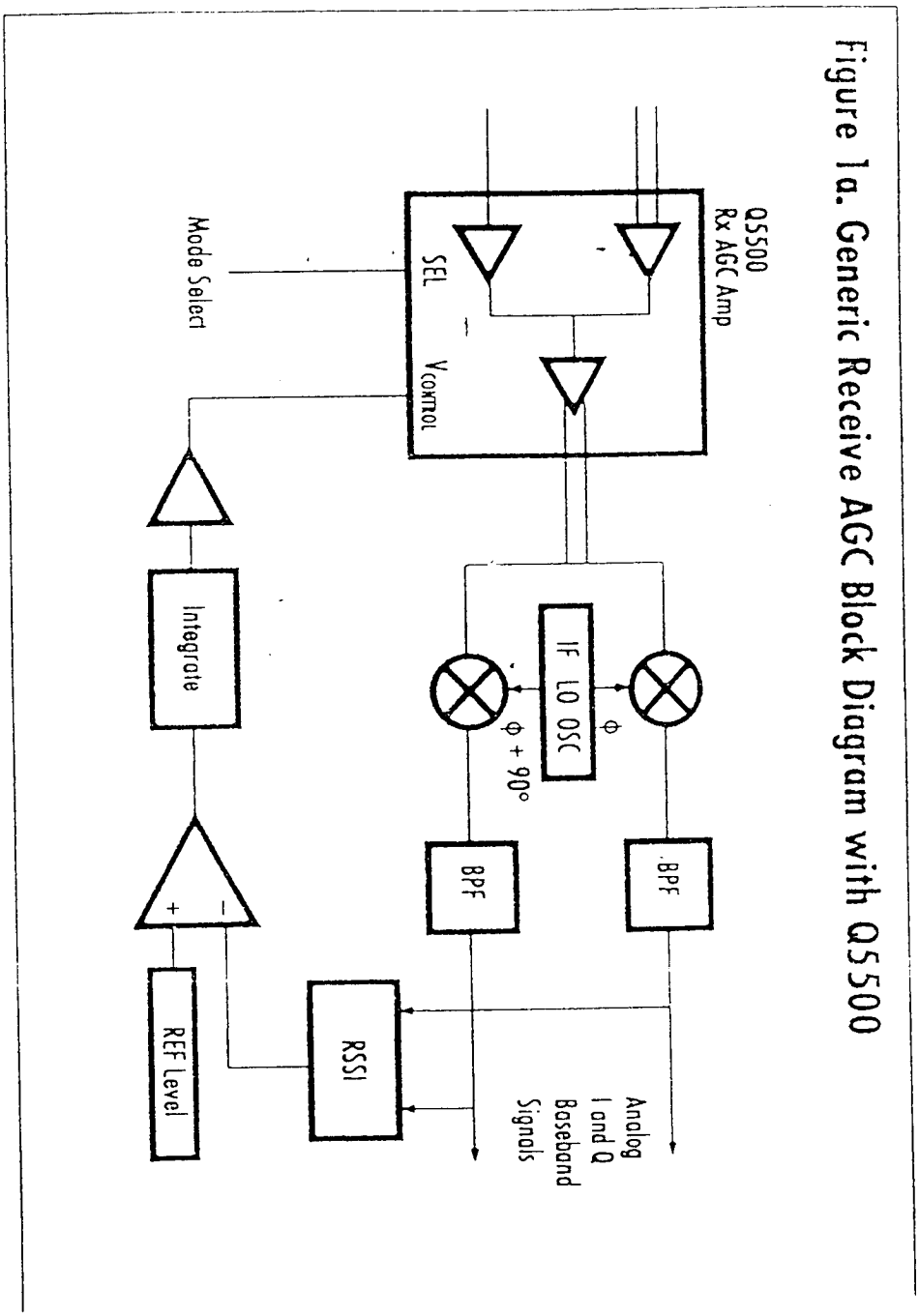


Figure 1a. Generic Receive AGC Block Diagram with Q5500

Table 1. Q5500 Specifications

PARAMETER[1]	MIN	TYP	MAX	UNITS	NOTES
Frequency Range	10	–	300	MHz	–
Maximum Gain @ $V_{CONTROL}$ = 3 V	+ 45	–	–	dB	2
Minimum Gain @ $V_{CONTROL}$ = 0.1 V	- 45	–	–	dB	2
Gain Variation in ± 630 KHz bandwidth centered at 85 MHz	–	± 0.05	–	dB	–
Gain Control Voltage Range (source impedance = 4.7 kΩ)	–	0.1 - 3	–	Vdc	2
Gain Control Input Impedance	–	60	–	kΩ	–
Noise Figure @ G = 45 dB (FM and CDMA Mode)	–	5	–	dB	2
FM Mode Input IP3 @ G = -45 dB	–	- 7	–	dBm	2
CDMA Mode Input IP3 @ G = -45 dB	–	- 3	–	dBm	2
CDMA Mode Input Resistance (differential)	–	1000	–	Ω	–
FM Mode Input Resistance (single-ended)	–	850	–	Ω	–
Input Capacitance (FM and CDMA mode)	–	1	–	pF	–
CDMA to FM Isolation	–	30	–	dB	–
Power Supply Voltage	–	3.6 ± 5%	–	V	–
FM Mode Current Consumption	–	11.3	–	mA	2
CDMA Mode Current Consumption	–	10.1	–	mA	2
Temperature Range (Case)	- 30	–	+ 80	°C	–

Notes:

1. Specified at 25° C, 85 MHz, V_{CC} = 3.6 V, Z_S = 500Ω, Z_L = 500 Ω, 1 KΩ External CDMA Input Terminating Resistor, 500 Ω External Output Terminating Resistor (Effective Z_S = 333 Ω, Effective Z_L = 250 Ω) Per Input/Output Loading of Figure 2.
2. See Typical Performance Characteristics in Figures 3 through 6.

Figure 2a. Definition of FM Source Impedance, Z_S, and Input Impedance, Z_{IN}, for Q5500

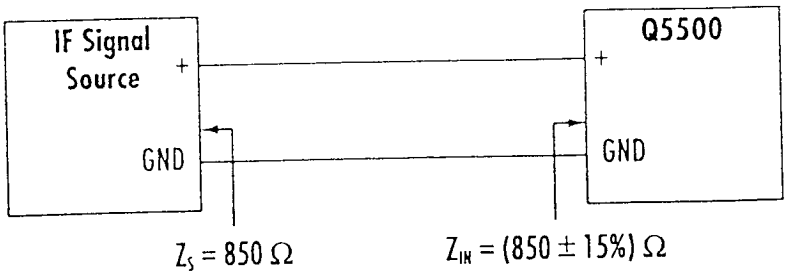


Figure 2b. Definition of CDMA Source Impedance, Z_S, and Input Impedance, Z_{IN}, for Q5500

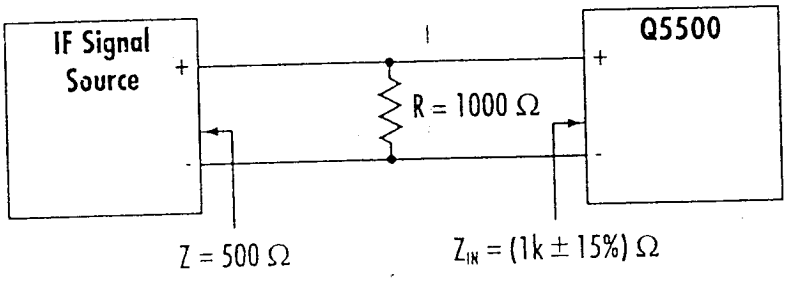
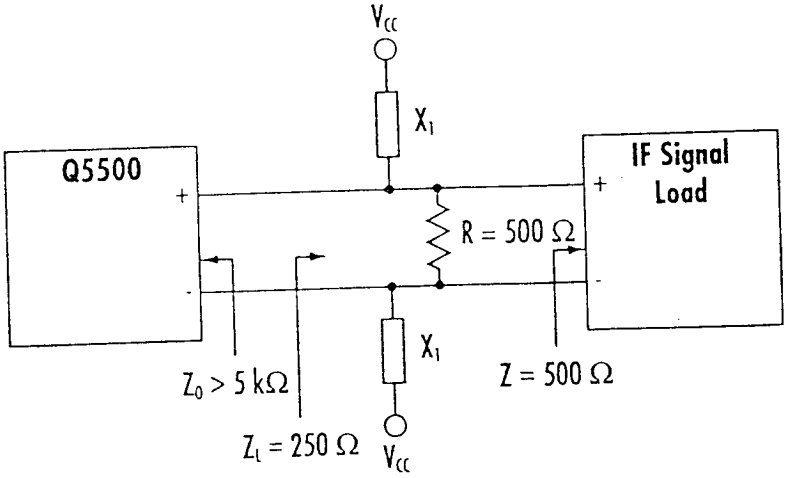


Figure 2c. Definition of Load Impedance, Z_L, and Output Impedance, Z_O, for Q5500



Note: X_1 can be a resistor or an inductor.
If it is a resistor, $X_1 = 250\ \Omega$ and the 500 Ω resistor will not be used
If it is an inductor, $L = 2.7\ \mu H$.

Table 2a-g. Description of Q5500 Pin Functions

a. CDMA Waveform Hi-Gain Digital Mode Differential Input Pin Functions

SYMBOL	PINS	I/O Type	FUNCTION
CDMA +	1	Differential Input	CDMA Positive Differential Input.
CDMA –	2	Differential Input	CDMA Negative Differential Input.

b. FM Waveform Low-Gain Analog Mode Single Ended Input Pin Functions

SYMBOL	PINS	I/O Type	FUNCTION
FM +	4	Single Ended AC Input	Single Ended Analog Input.

Analog Gain Control Input Pin Functions

SYMBOL	PINS	I/O Type	FUNCTION
$V_{CONTROL}$	16	DC Input	$V_{CONTROL}$ – Analog Gain Control Input. $V_{CONTROL}$ = 0.1 V, Low Gain Rail. $V_{CONTROL}$ = 3.0 V, High Gain Rail.

d. Analog/Digital Mode Select Input Pin Functions

SYMBOL	PINS	I/O Type	FUNCTION
SEL	7	CMOS Input	$V_{SELECT} \geq +3.4$ V, Digital Mode Select. $V_{SELECT} \leq +0.5$ V, Analog Mode Select.

e. Analog Differential Output Pin Functions

SYMBOL	PINS	I/O Type	FUNCTION
OUT +	10	Differential Output	Analog Positive Differential Output.
OUT –	9	Differential Output	Analog Negative Differential Output.

f. Unconnected Pin Functions

SYMBOL	PINS	I/O Type	FUNCTION
–	8	N/C	Unconnected Pin.

g. Voltage Supply Pin Functions

SYMBOL	PINS	I/O Type	FUNCTION
V_{CC}	13, 14, 15	Power	V_{CC} Power Supply.
GND	3, 6, 11, 12	Ground	Ground Connection.
AC GND	5	AC Ground	Analog Ground Connection.

Figure 7. Q5500 Functional Block Diagram

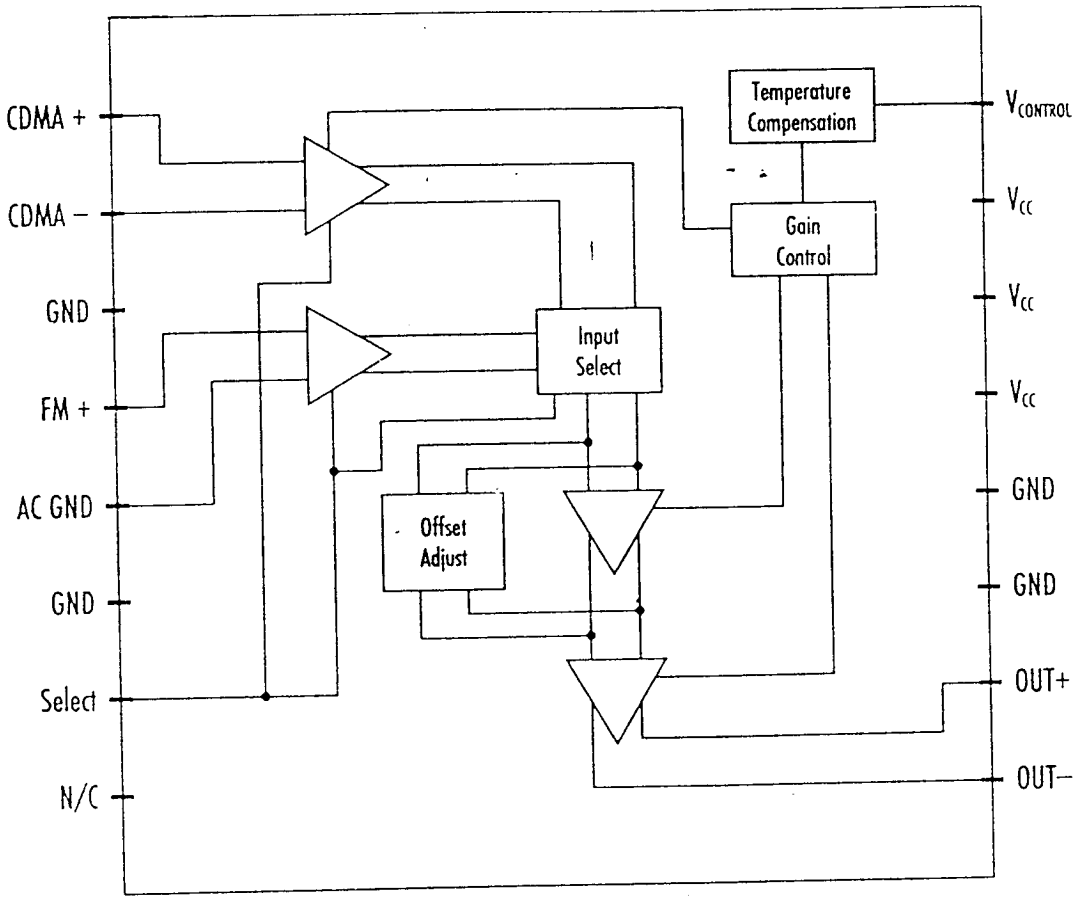


Figure 1b. Generic Transmit AGC Block Diagram with Q5505

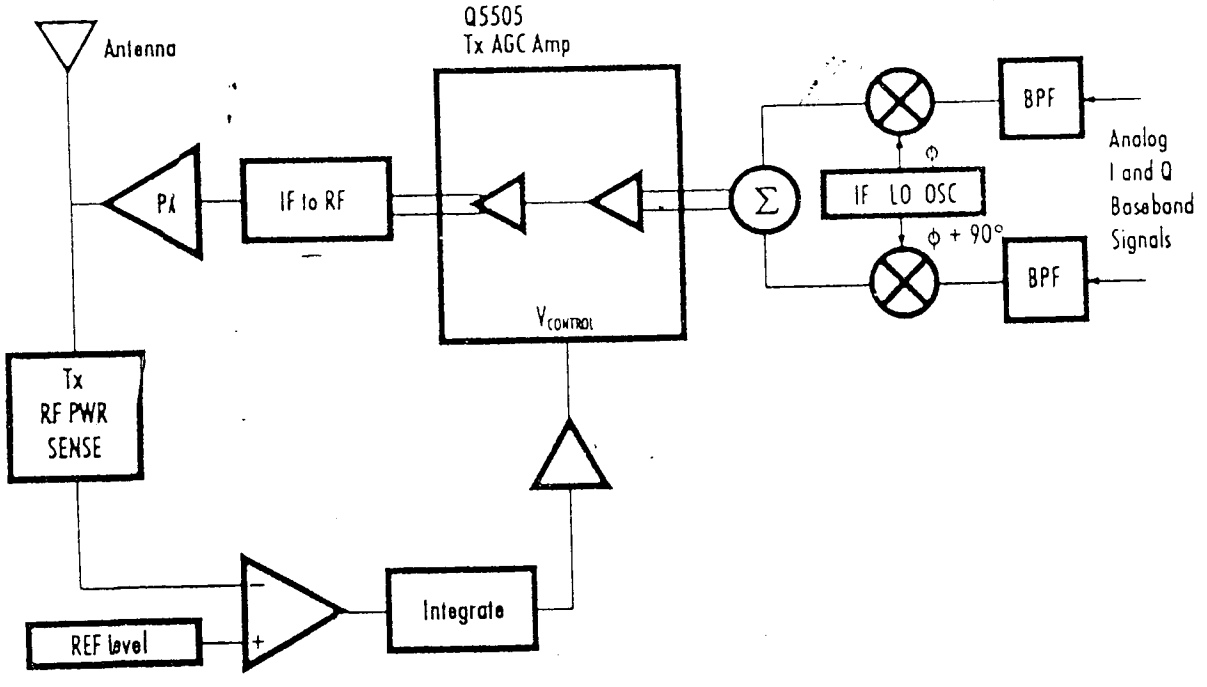


Table 3. Q5505 Specifications

PARAMETER[1]	MIN	TYP	MAX	UNITS	NOTES
Frequency Range	10	–	250	MHz	–
Maximum Gain @ $V_{CONTROL}$ = 3 V	+ 39	–	–	dB	2
Minimum Gain @ $V_{CONTROL}$ = 0.1 V	- 45	–	–	dB	2
Gain Variation in ± 630 KHz bandwidth centered at 130 MHz	–	± 0.05	–	dB	–
Gain Control Voltage Range	–	0.1 - 3	–	Vdc	2
Gain Control Input Impedance	–	60	–	kΩ	–
Noise Figure @ G = 39 dB	–	5	–	dB	2
Output IP3 @ G = 35 dB (Referenced to 1000 Ω)	–	20	–	dBm	2
Input Impedance (CDMA differential)	–	1000	–	Ω	–
Power Supply Voltage	–	3.6 ± 5%	–	V	–
Current Consumption (@ $V_{CONTROL}$ = 3 V)	–	20	–	mA	2
Temperature Range (Case)	- 30	–	+ 80	°C	–

Notes:

1. Specified at 25° C, 130 MHz, V_{CC} = 3.6 V, Z_S = 1000Ω, Z_L = 1000 Ω, 1 KΩ External Output Terminating Resistor, (Effective Z_L = 500 Ω)
   Per Input/Output Loading of Figure 9.
2. See Typical Performance Characteristics in Figures 10 and 11.

Figure 9a. Definition of Source Impedance, Z_S, and Input Impedance, Z_{IN}, for Q5505.

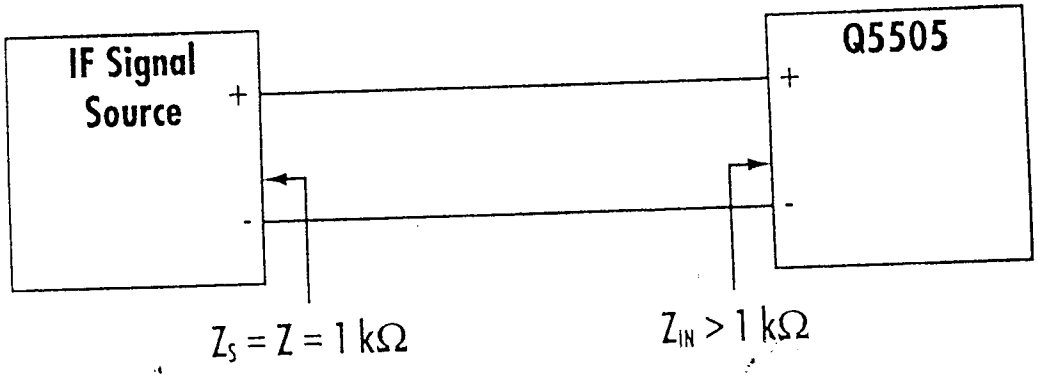


Figure 9b. Definition of Load Impedance, Z_L, and Output Impedance, Z_O, for Q5505.

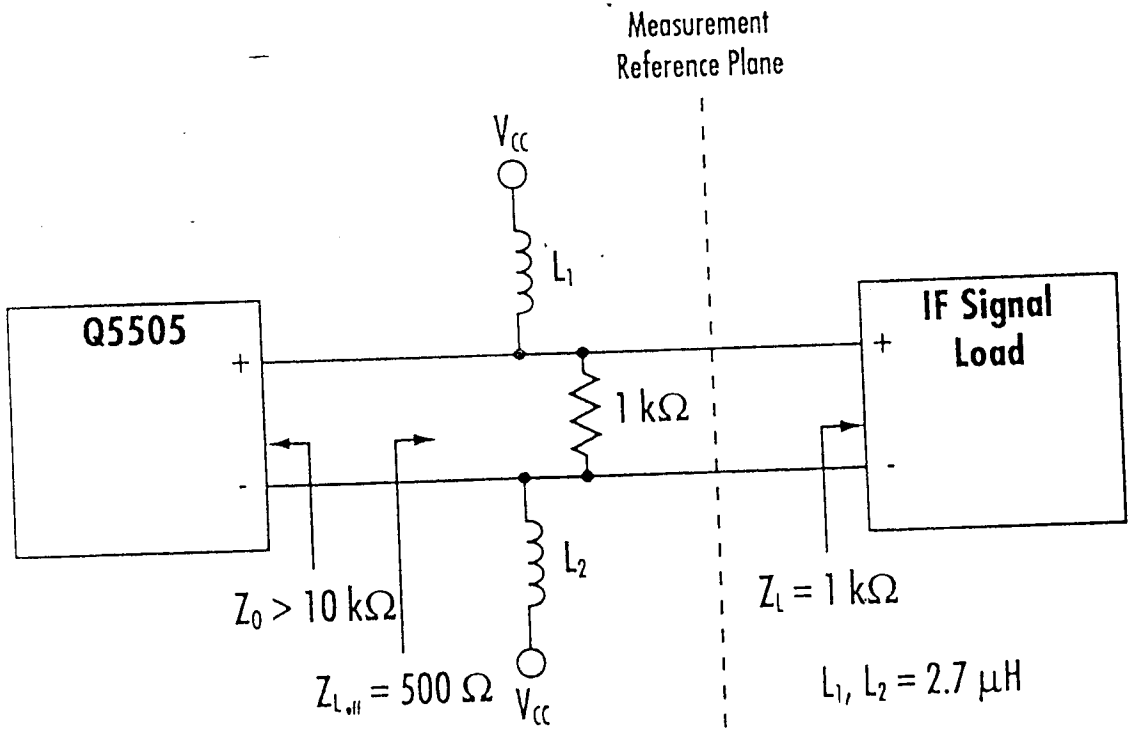


Table 4a-e. Description of Q5505 Pin Functions

a. CDMA Waveform Hi-Gain Digital Mode Differential Input Pin Functions

SYMBOL	PINS	I/O Type	FUNCTION
CDMA +	1	Differential Input	CDMA Positive Differential Input.
CDMA –	2	Differential Input	CDMA Negative Differential Input.

b. Analog Gain Control Input Pin Functions

SYMBOL	PINS	I/O Type	FUNCTION
$V_{CONTROL}$	16	DC Input	$V_{CONTROL}$ – Analog Gain Control Input. $V_{CONTROL}$ = 0.1 V, Low Gain Rail. $V_{CONTROL}$ = 3.0 V, High Gain Rail.

c. Analog Differential Output Pin Functions

SYMBOL	PINS	I/O Type	FUNCTION
OUT +	10	Differential Output	Analog Positive Differential Output.
OUT –	9	Differential Output	Analog Negative Differential Output.

d. Unconnected Pin Functions

SYMBOL	PINS	I/O Type	FUNCTION
–	8	N/C	Unconnected Pin.

e. Voltage Supply Pin Functions

SYMBOL	PINS	I/O Type	FUNCTION
V_{CC}	13, 14, 15	Power	V_{CC} Power Supply.
GND	3, 4, 5, 6, 7, 11, 12	Ground	Ground Connection.

Figure 12. Q5505 Functional Block Diagram

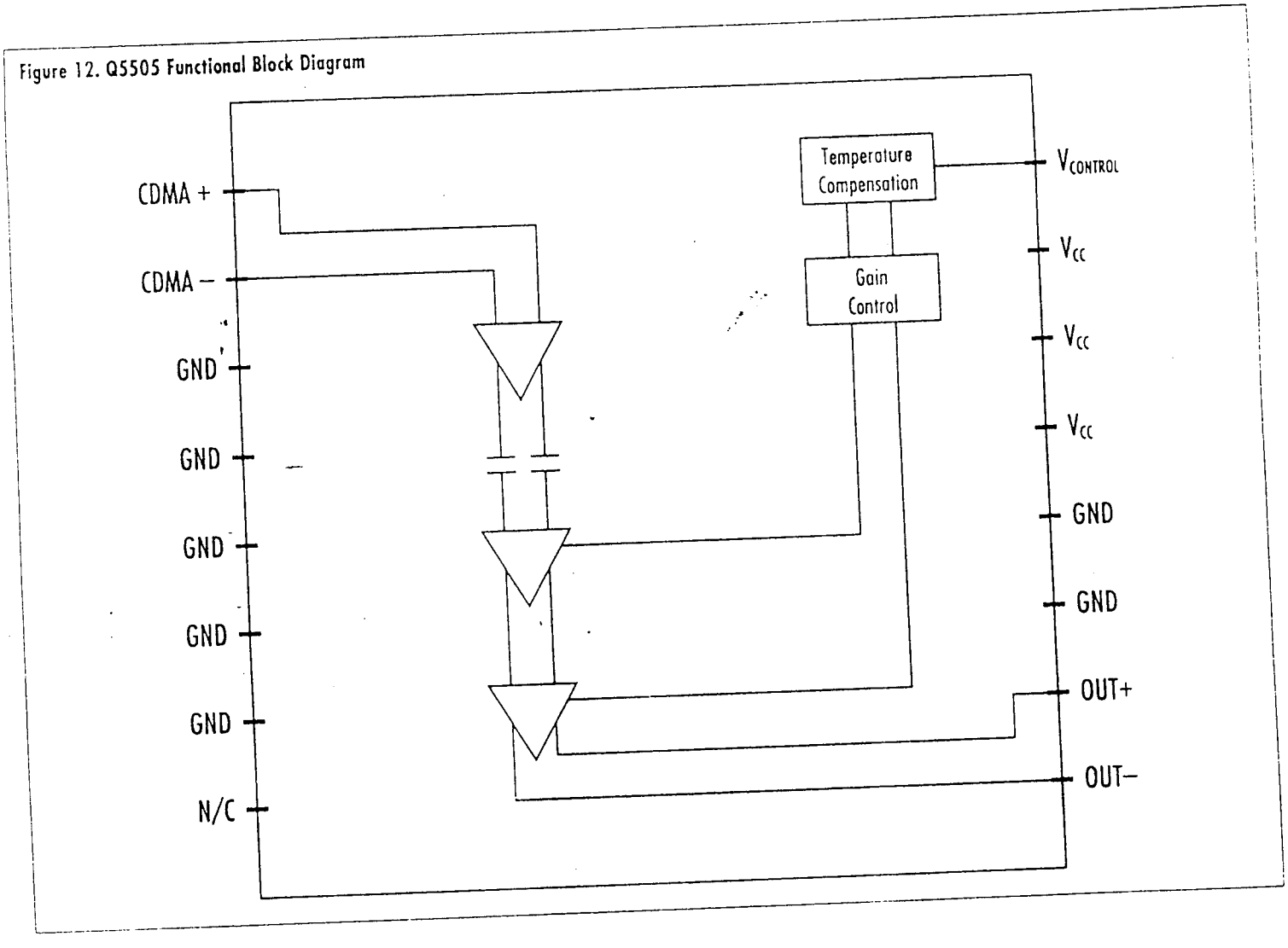


Table 5. Order Information

PART NUMBER	DESCRIPTION	DEVICE CARRIER
Q5500I-1M	Receive Variable Gain Amplifier	Plastic Tube
Q5500I-1M-TR	Receive Variable Gain Amplifier	Tape and Reel
Q5505I-1M	Transmit Variable Gain Amplifier	Plastic Tube
Q5505I-1M-TR	Transmit Variable Gain Amplifier	Tape and Reel

Audio Processor

SGS-THOMSON MICROELECTRONICS

ST5092

2.7V SUPPLY 14-BIT LINEAR CODEC WITH HIGH-PERFORMANCE AUDIO FRONT-END

PRELIMINARY DATA

FEATURES:

Complete CODEC and FILTER system including:

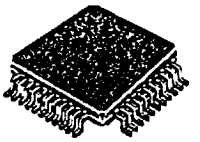
- 14 BIT LINEAR ANALOG TO DIGITAL AND DIGITAL TO ANALOG CONVERTERS.
- 8 BIT COMPANDED ANALOG TO DIGITAL AND DIGITAL TO ANALOG CONVERTERS A-LAW OR μ-LAW.
- TRANSMIT AND RECEIVE BAND-PASS FILTERS
- ACTIVE ANTIALIAS NOISE FILTER.

Phone Features:

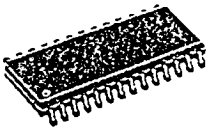
- THREE SWITCHABLE MICROPHONE AMPLIFIER INPUTS. GAIN PROGRAMMABLE: 20 dB PREAMP. (+MUTE), 0 . . 22.5 dB AMPLIFIER, 1.5 dB STEPS.
- EARPIECE AUDIO OUTPUT. ATTENUATION PROGRAMMABLE: 0 . . 30 dB, 2 dB STEPS.
- EXTERNAL AUDIO OUTPUT. ATTENUATION PROGRAMMABLE: 0 . . 30 dB, 2 dB STEPS.
- TRANSIENT SUPRESSION SIGNAL DURING POWER ON AND DURING AMPLIFIER SWITCHING.
- INTERNAL PROGRAMMABLE SIDETONE CIRCUIT. ATTENUATION PROGRAMMABLE: 16 dB RANGE, 1 dB STEP. ROUTING POSSIBLE TO BOTH OUTPUTS.
- INTERNAL RING OR TONE GENERATOR INCLUDING DTMF TONES, SINEWAVE OR SQUAREWAVE WAVEFORMS. ATTENUATION PROGRAMMABLE: 27dB RANGE, 3dB STEP. THREE FREQUENCY RANGES:
  a) 3.9Hz . . . . 996Hz, 3.9Hz STEP
  b) 7.8Hz . . . . 1992Hz, 7.8Hz STEP
  c) 15.6Hz . . . . 3984Hz, 15.6Hz STEP
- PROGRAMMABLE PULSE WIDTH MODULATED BUZZER DRIVER OUTPUT.

General Features:

- SINGLE 2.7V to 3.6V SUPPLY
- EXTENDED TEMPERATURE RANGE OPERATION (*) -40°C to 85°C.
- 1.5 μW STANDBY POWER (TYP. AT 3.0V).
- 15mW OPERATING POWER (TYP. AT 3.0V).
- 13mW OPERATING POWER (TYP. AT 2.7V).
- CMOS COMPATIBLE DIGITAL INTERFACES.
- PROGRAMMABLE PCM AND CONTROL INTERFACE MICROWIRE COMPATIBLE.



TQFP44(10x10x1.4)



SO28

ORDERING NUMBERS:

	Package	Dim.	Cond.
ST5092AD	SO28		Tube
ST5092ADTR	SO28		Tape&Reel
ST5092TQFP	TQFP44	10x10x1.4	Tray 8x20
ST5092TQFPTR	TQFP44	10x10x1.4	Tape&Reel

APPLICATIONS:

- GSM DIGITAL CELLULAR TELEPHONES.
- CT2 DIGITAL CORDLESS TELEPHONES.
- DECT DIGITAL CORDLESS TELEPHONES.
- BATTERY OPERATED AUDIO FRONT-ENDS FOR DSPs.

(*) Functionality guaranteed in the range – 40°C to +85°C; Timing and Electrical Specifications are guaranteed in the range –30°C to +85°C.

GENERAL DESCRIPTION

ST5092 is a high performance low power combined PCM CODEC/FILTER device tailored to implement the audio front-end functions required by the next generation low voltage/low power consumption digital terminals.

ST5092 offers a number of programmable functions accessed through a serial control channel that easily interfaces to any classical microcontroller.

The PCM interface supports both non-delayed (normal and reverse) and delayed frame synchronization modes.

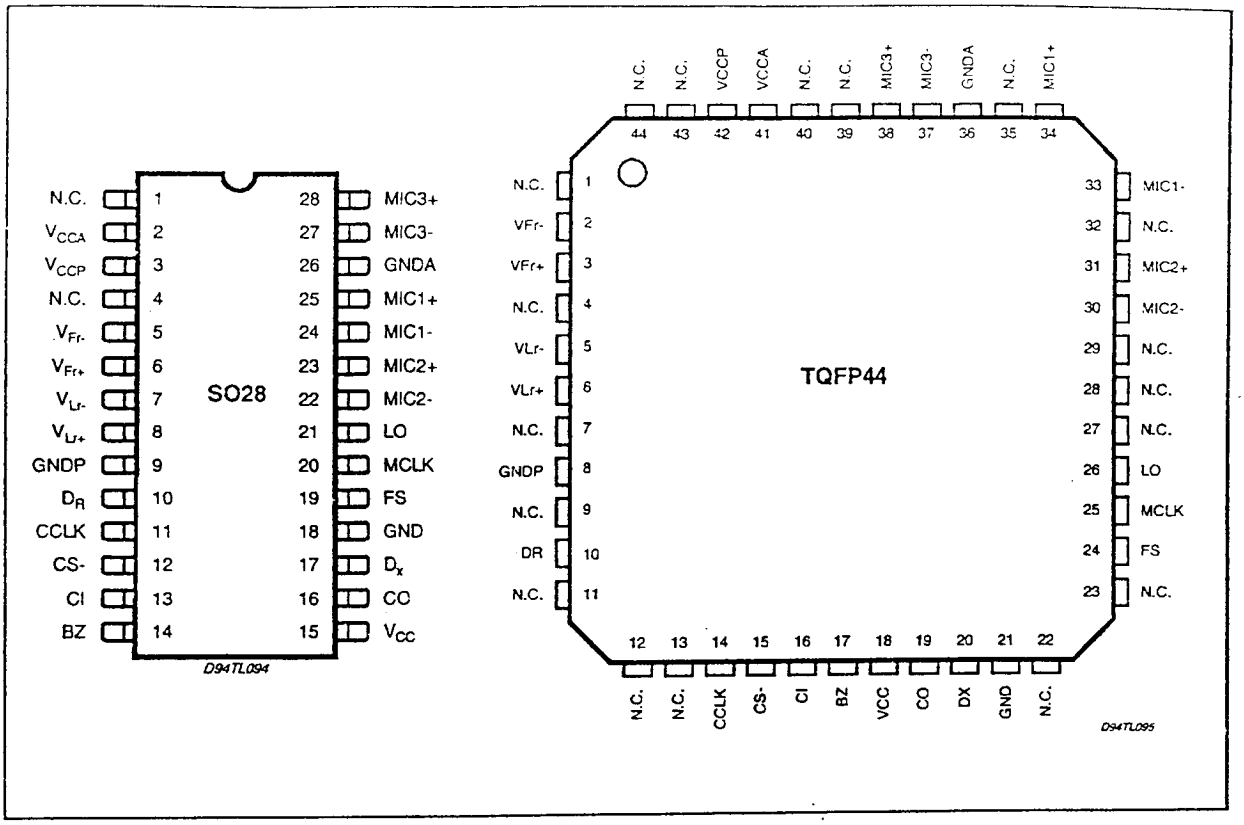
ST5092 can be configurated either as a 14-bit linear or as an 8-bit companded PCM coder.

Additionally to the CODEC/FILTER function, ST5092 includes a Tone/Ring/DTMF generator, a sidetone generation, and a buzzer driver output.

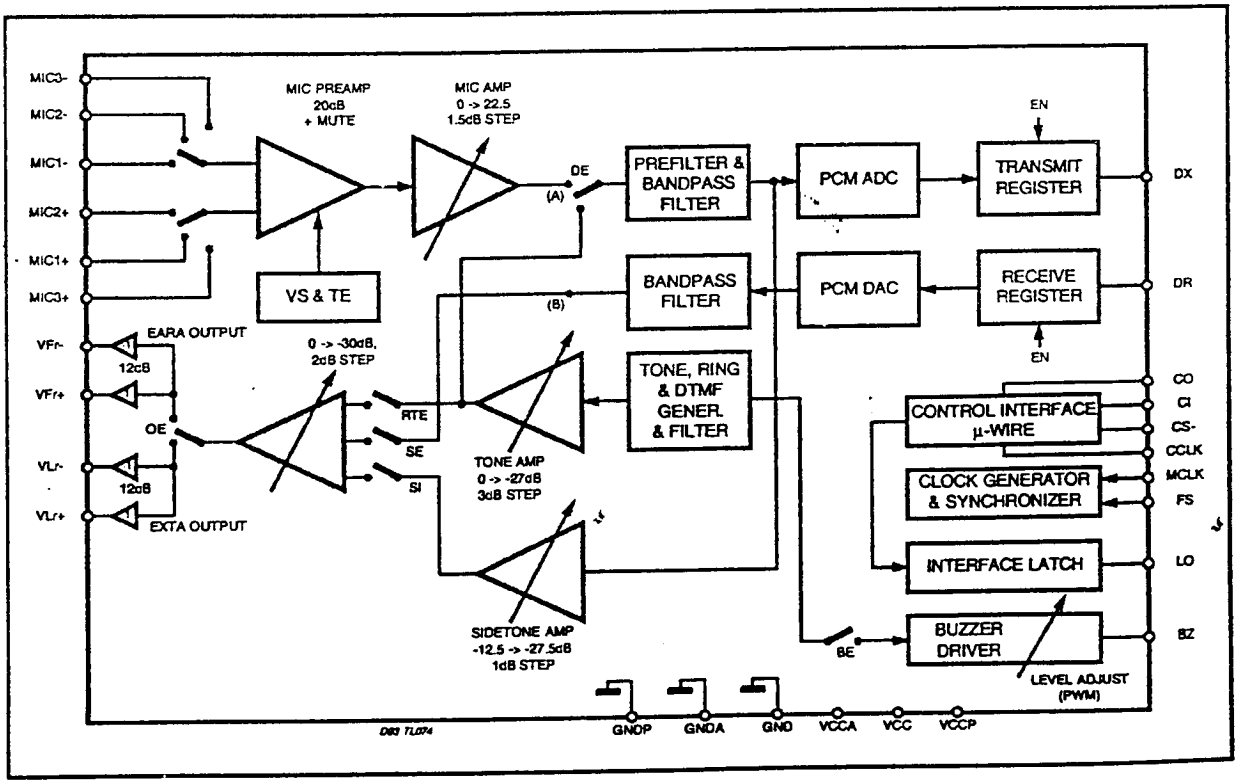
ST5092 fulfils and exceeds D3/D4 and CCITT recommendations and ETSI requirements for digital handset terminals.

Main applications include digital mobile phones, as cellular and cordless phones, or any battery powered equipment that requires audio codecs operating at low single supply voltages

PIN CONNECTIONS (Top view)



BLOCK DIAGRAM



PIN FUNCTIONS (SO28)

Pin	Name	Description
1	N.C.	Not Connected.
2	V_{CCA}	Positive power supply input for the analog section. V_{CC} and V_{CCA} must be directly connected together.
3	V_{CCP}	Positive power supply input for the power section. V_{CCP} and V_{CC} must be connected together.
4	N.C.	Not Connected.
5,6	V_{Fr+}, V_{Fr-}	Receive analog earpiece amplifier complementary outputs. These outputs can drive directly earpiece transductor. The signal at this output can be the sum of: - Receive Speech signal from D_R, - Internal Tone Generator, - Sidetone signal.
7,8	V_{Lr+}, V_{Lr-}	Receive analog extra amplifier complementary outputs. The signal at these outputs can be the sum of: - Receive Speech signal from DR, - Internal Tone generator, - Sidetone signal.
9	GNDP	Power ground. V_{Fr} and V_{Lr} driver are referenced to this pin. GNDP and GND must be connected together close to the device.
10	D_R	Receive data input: Data is shifted in during the assigned Received time slots In delayed and non-delayed normal frame synchr. modes voice data byte is shifted in at the MCLK frequency on the falling edges of MCLK, while in non-delayed reverse frame synchr. mode voice data byte is shifted in at the MCLK frequency on the rising edges of MCLK.
11	CCLK	Control Clock input: This clock shifts serial control information into CI and out from CO when the CS- input is low, depending on the current instruction. CCLK may be asynchronous with the other system clocks.
12	CS-	Chip Select input: When this pin is low, control information is written into and out from the ST5092 via CI and CO pins.
13	CI	Control data Input: Serial Control information is shifted into the ST5092 on this pin when CS- is low on the rising edges of CCLK.
14	BZ	Pulse width modulated buzzer driver output.
15	V_{CC}	Positive power supply input for the digital section.
16	CO	Control data Output: Serial control/status information is shifted out from the ST5092 on this pin when CS- is low on the falling edges of CCLK.
17	D_X	Transmit Data ouput: Data is shifted out on this pin during the assigned transmit time slots. Elsewhere D_X output is in the high impedance state. In delayed and non-delayed normal frame synchr. modes, voice data byte is shifted out from TRISTATE output D_X at the MCLK on the rising edge of MCLK, while in non-delayed reverse frame synchr mode voice data byte is shifted out on the falling edge of MCLK.
18	GND	Ground: All digital signals are referenced to this pin.
19	FS	Frame Sync input: This signal is a 8kHz clock which defines the start of the transmit and receive frames. Any of three formats may be used for this signal: non delayed normal mode, delayed mode, and non delayed reverse mode.
20	MCLK	Master Clock Input: This signal is used by the switched capacitor filters and the encoder/decoder sequencing logic. Values must be 512 kHz, 1.536 MHz, 2.048 MHz or 2.56 MHz selected by means of Control Register CRO. MCLK is used also to shift-in and out data.
21	LO	A logic 1 written into DO (CR1) appears at LO pin as a logic 0 A logic 0 written into DO (CR1) appears at LO pin as a logic 1.
22	MIC2-	Second negative high impedance input to transmit pre-amplifier for microphone connection.
23	MIC2+	Second Positive high impedance input to transmit pre-amplifier for microphone connection.
24	MIC1-	Negative high impedance input to transmit pre-amplifier for microphone connection.
25	MIC1+	Positive high impedance input to transmit pre-amplifier for microphone connection.
26	GNDA	Analog Ground: All analog signals are referenced to this pin. GND and GNDA must be connected together close to the device.
27	MIC3-	Third negative high impedance output to transmit preamplifier for microphone connection.
28	MIC3+	Third positive high impedance output to transmit preamplifier for microphone connection.

PIN FUNCTIONS (TQFP44)

Pin	Name	Description
1	N.C.	Not Connected.
2,3	V_{Fr+}, V_{Fr-}	Receive analog earpiece amplifier complementary outputs. These outputs can drive directly earpiece transductor. The signal at this output can be the summ of: - Receive Speech signal from D_R, - Internal Tone Generator, - Sidetone signal.
4	N.C.	Not Connected.
5,6	V_{Lr+}, V_{Lr-}	Receive analog extra amplifier complementary outputs. The signal at these outputs can be the sum of: - Receive Speech signal from DR, - Internal Tone generator, - Sidetone signal.
7	N.C.	Not Connected.
8	GNDP	Power ground. V_{Fr} and V_{Lr} driver are referenced to this pin. GNDP and GND must be connected together close to the device.
9	N.C.	Not Connected.
10	D_R	Receive data input: Data is shifted in during the assigned Received time slots In delayed and non-delayed normal frame synchr. modes voice data byte is shifted in at the MCLK frequency on the falling edges of MCLK, while in non-delayed reverse frame sinchr. mode voice data byte is shifted in at the MCLK frequency on the rising edges of MCLK.
11,12,13	N.C.	Not Connected.
14	CCLK	Control Clock input: This clock shifts serial control information into CI and out from CO when the CS- input is low, depending on the current instruction. CCLK may be asynchronous with the other system clocks.
15	CS-	Chip Select input: When this pin is low, control information is written into and out from the ST5092 via CI and CO pins.
16	CI	Control data Input: Serial Control information is shifted into the ST5092 on this pin when CS- is low on the rising edges of CCLK.
17	BZ	Pulse width modulated buzzer driver output.
18	V_{CC}	Positive power supply input for the digital section.
19	CO	Control data Output: Serial control/status information is shifted out from the ST5092 on this pin when CS- is low on the falling edges of CCLK.
20	D_X	Transmit Data ouput: Data is shifted out on this pin during the assigned transmit time slots. Elsewhere D_X output is in the high impendance state. In delayed and non-delayed normal frame synchr. modes, voice data byte is shifted out from TRISTATE output D_X at the MCLK on the rising edge of MCLK, while in non-delayed reverse frame synchr mode voice data byte is shifted out on the falling edge of MCLK.
21	GND	Ground: All digital signals are referenced to this pin.
22,23	N.C.	Not Connected.
24	FS	Frame Sync input: This signal is a 8kHz clock which defines the start of the transmit and receive frames. Either of three formats may be used for this signal: non delayed normal mode, delayed mode, and non delayed reverse mode.
25	MCLK	Master Clock Input: This signal is used by the switched capacitor filters and the encoder/decoder sequencing logic. Values must be 512 kHz, 1.536 MHz, 2.048 MHz or 2.56 MHz selected by means of Control Register CR0. MCLK is used also to shift-in and out data.
26	LO	A logic 1 written into DO (CR1) appears at LO pin as a logic 0 A logic 0 written into DO (CR1) appears at LO pin as a logic 1.
27,28,29	N.C.	Not Connected.
30	MIC2-	Second negative high impedance input to transmit pre-amplifier for microphone connection.
31	MIC2+	Second Positive high impedance input to transmit pre-amplifier for microphone connection.
32	N.C.	Not Connected.
33	MIC1-	Negative high impedance input to transmit pre-amplifier for microphone connection.
34	MIC1+	Positive high impedance input to transmit pre-amplifier for microphone connection.
35	N.C.	Not Connected.
36	GNDA	Analog Ground: All analog signals are referenced to this pin. GND and GNDA must be connected together close to the device.
37	MIC3-	Third negative high impedance output to transmit preamplifier for microphone connection.
38	MIC3+	Third positive high impedance output to transmit preamplifier for microphone connection.
39,40	N.C.	Not Connected.
41	V_{CCA}	Positive power supply input for the analog section. V_{CC} and V_{CCA} must be directly connected together.
42	V_{CCP}	Positive power supply input for the power section. V_{CCP} and V_{CC} must be connected together.
43,44	N.C.	Not Connected.

FUNCTIONAL DESCRIPTION

I DEVICE OPERATION

I.1 **Power on initialization:**

When power is first applied, power on reset circuitry initializes ST5092 and puts it into the power down state. Gain Control Registers for the various programmable gain amplifiers and programmable switches are initialized as indicated in the Control Register description section. All CODEC functions are disabled.

The desired selection for all programmable functions may be intialized prior to a power up command using the MICROWIRE control channel.

I.2 **Power up/down control:**

Following power-on initialization, power up and power down control may be accomplished by writing any of the control instructions listed in Table 1 into ST5092 with "P" bit set to 0 for power up or 1 for power down.

Normally, it is recommended that all programmable functions be initially programmed while the device is powered down. Power state control can then be included with the last programming instruction or in a separate single byte instruction.

Any of the programmable registers may also be modified while ST5092 is powered up or down by setting "P" bit as indicated. When power up or down control is entered as a single byte instruction, bit 1 must be set to a 0.

When a power up command is given, all de-activated circuits are activated, but output Dx will remain in the high impedance state until the second Fs pulse after power up.

I.3 **Power down state:**

Following a period of activity, power down state may be reentered by writing a power down instruction.

Control Registers remain in their current state and can be changed by MICROWIRE control interface.

In addition to the power down instruction, detection of loss MCLK (no transition detected) automatically enters the device in "reset" power down state with Dx output in the high impedance state.

I.4 **Transmit section:**

Transmit analog interface is designed in two stages to enable gains up to 42.5 dB to be realized. Stage 1 is a low noise differential amplifier providing 20 dB gain. A microphone may be capacitevely connected to MIC1+, MIC1- inputs, while the MIC2+ MIC2– and MIC3+ MIC3- inputs may be used to capacitively connect a second microphone or a third microphone respectively or an auxiliary audio circuit. MIC1 or MIC2 or MC3 or transmit mute is selected with bits 6 and 7 of register CR4.

In the mute case, the analog transmit signal is grounded and the sidetone path is also disabled. Following the first stage is a programmable gain amplifier which provides from 0 to 22.5 dB of additional gain in 1.5dB step. The total transmit gain should be adjusted so that, at reference point A, see Block Diagram description, the internal 0 dBm0 voltage is 0.49 Vrms (overload level is 0.7 Vrms). Second stage amplifier gain can be programmed with bits 4 to 7 of CR5.

An active RC prefilter then precedes the 8th order band pass switched capacitor filter. A/D converter can be either a 14-bit linear (bit CM = 0 in register CR0) or can have a compressing characteristics (bit CM = 1 in register CR0) according to CCITT A or MU255 coding laws. A precision on chip voltage reference ensures accurate and highly stable transmission levels.

Any offset voltage arising in the gain-set amplifier, the filters or the comparator is cancelled by an internal autozero circuit.

Each encode cycle begins immediatly at the beginning of the selected Transmit time slot. The total signal delay referenced to the start of the time slot is approximatively 195 µs (due to the transmit filter) plus 125 µs (due to encoding delay), which totals 320 µs. Voice data is shifted out on Dx during the selected time slot on the transmit rising edges of MCLK in delayed or non-delayed normal mode or on the falling edges of MCLK in non-delayed reverse mode.

I.5 **Receive section:**

Voice Data is shifted into the decoder's Receive voice data Register via the D_R pin during the selected time slot on the falling edges of MCLK in delayed or non-delayed normal mode or on the rising edges of MCLK in non-delayed reverse mode.

The decoder consists of either a 14-bit linear or an expanding DAC with A or MU255 law decoding characteristic. Following the Decoder is a 3400 Hz 8th order band-pass switched capacitor filter with integral Sin X/X correction for the 8 kHz sample and hold.

0 dBmO voltage at this (B) reference point (see Block Diagram description) is 0.49 Vrms. A transcient suppressing circuitry ensure interference noise suppression at power up.

The analog speech signal output can be routed either to earpiece (V_{FR+}, V_{FR-} outputs) or to an extra analog output (V_{LT+}, V_{LT-} outputs) by setting bits OE and SE (1 and 0 of CR4).

Total signal delay is approximatively 190 µs (filter plus decoding delay) plus 62.5 µs (1/2 frame) which gives approximatively 252 µs.

Differential outputs V_{FR+},V_{FR-} are intended to directly drive an earpiece. Preceding the outputs is a programmable attenuation amplifier, which must

be set by writing to bits 4 to 7 in register CR6. Attenuations in the range 0 to -30 dB relative to the maximum level in 2 dB step can be programmed. The input of this programmable amplifier is the sum of several signals which can be selected by writing to register CR4.:

- Receive speech signal which has been decoded and filtered,
- Internally generated tone signal, (Tone amplitude is programmed with bits 4 to 7 of register CR7),
- Sidetone signal, the amplitude of which is programmed with bits 0 to 3 of register CR5

V_{FR+} and V_{FR-} outputs are capable of driving output power level up to 66mW into differentially connected load impedance of 30 Ω. Piezoceramic receivers up to 50nF can also be driven.

Differential outputs V_{LT+},V_{LT-} are intended to directly drive an extra output. Preceding the outputs is a programmable attenuation amplifier, which must be set by writing to bits 0 to 3 in register CR6. Attenuations in the range 0 to -30 dB relative to the maximum level in 2.0 dB step can be programmed. The input of this programmable amplifier can be the sum of signals which can be selected by writing to register CR4:

- Receive speech signal which has been decoded and filtered,
- Internally generated tone signal, (Tone amplitude is programmed with bits 4 to 7 of register CR7),
- Sidetone signal, the amplitude of which is programmed with bits 0 to 3 of register CR5.

V_{LT+} and V_{LT-} outputs are capable of driving output power level up to 66mW into differentially connected load impedance of 30 Ω. Piezoceramic receivers up to 50nF can also be driven.

BUZZER OUTPUT:
Single ended output BZ is intended to drive a buzzer, via an external BJT, with a squarewave pulse width modulated (PWM) signal the frequency of which is stored into register CR8.
For some applications it is also possible to amplitude modulate this PWM signal with a squarewave signal having a frequency stored in register CR9.
Maximum load for BZ is 5kΩ and 50pF.

I.6 Digital Interface (Fig. 1)

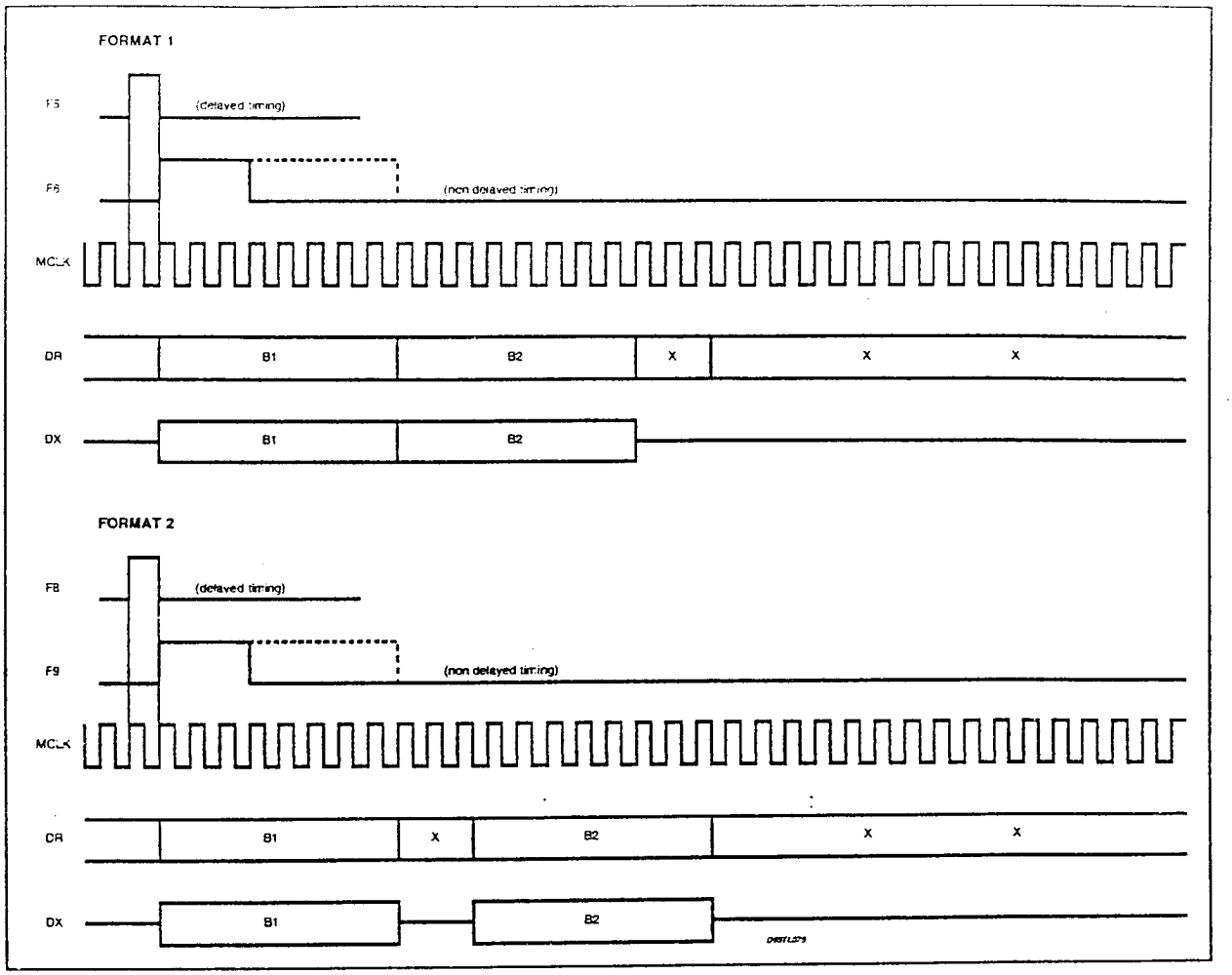
F_S Frame Sync input determines the beginning of frame. It may have any duration from a single cycle of MCLK to a squarewave. Three different relationships may be established between the Frame Sync input and the first time slot of frame by setting bits DM1 and DM0 in register CR1.

Non delayed data mode is similar to long frame timing on ST5080A: first time slot begins nominally coincident with the rising edge of F_S. Alternative is to use delayed data mode, which is similar to short frame sync timing on ST5080A, in which F_S input must be high at least a half cycle of MCLK earlier the frame beginning. In the case of companded code only (bit CM = 1 in register CR0) a time slot assignment circuit on chip may be used with all timing modes, allowing connection to one of the two B1 and B2 voice data channels.
Two data formats are available: in Format 1, time slot B1 corresponds to the 8 MCLK cycles following immediately the rising edge of FS, while time slot B2 corresponds to the 8 MCLK cycles following immediately time slot B1.
In Format 2, time slot B1 is identical to Format 1. Time slot B2 appears two bit slots after time slot B1. This two bits space is left available for insertion of the D channel data.
Data format is selected by bit FF (2) in register CR0. Time slot B1 or B2 is selected by bit TS (1) in Control Register CR1.
Bit EN (2) in control register CR1 enables or disables the voice data transfer on D_X and D_R as appropriate. During the assigned time slot, D_X output shifts data out from the voice data register on the rising edges of MCLK in the case of delayed and non-delayed normal modes or on the falling edges of MCLK in the case of non-delayed reverse mode. Serial voice data is shifted into D_R input during the same time slot on the falling edges of MCLK in the case of delayed and non-delayed normal modes or on the rising edges of MCLK in the case of non-delayed reverse mode.
D_X is in the high impedance Tristate condition when in the non selected time slots.

I.7 Control Interface:

Control information or data is written into or read-back from ST5092 via the serial control port consisting of control clock CCLK, serial data input CI and output CO, and Chip Select input, CS-. All control instructions require 2 bytes as listed in Table 1, with the exception of a single byte power-up/down command.
To shift control data into ST5092, CCLK must be pulsed high 8 times while CS- is low. Data on CI input is shifted into the serial input register on the rising edge of each CCLK pulse. After all data is shifted in, the content of the input shift register is decoded, and may indicate that a 2nd byte of control data will follow. This second byte may either be defined by a second byte-wide CS- pulse or may follow the first contiguously, i.e. it is not mandatory for CS- to return high in between the first and second control bytes. At the end of the 2nd control byte, data is loaded into the ap-

Figure 1: Digital Interface Format (*)



(*) Significant Only For Companded Code.

propriate programmable register. CS- must return high at the end of the 2nd byte.
To read-back status information from ST5092, the first byte of the appropriate instruction is strobed in during the first CS- pulse, as defined in Table 1. CS- must be set low for a further 8 CCLK cycles, during which data is shifted out of the CO pin on the falling edges of CCLK.
When CS- is high, CO pin is in the high impedance Tri-state, enabling CO pins of several devices to be multiplexed together.
Thus, to summarise, 2 byte READ and WRITE instructions may use either two 8-bit wide CS- pulses or a single 16 bit wide CS- pulse.

I.8 **Control channel access to PCM interface:**
It is possible to access the B channel previously selected in Register CR1 in the case of companded code only.
A byte written into Control Register CR3 will be automatically transmitted from D_X output in the following frame in place of the transmit PCM data.
A byte written into Control Register CR2 will be automatically sent through the receive path to the Receive amplifiers.
In order to implement a continuous data flow from the Control MICROWIRE interface to a B channel, it is necessary to send the control byte on each PCM frame.
A current byte received on D_R input can be read in the register CR2. In order to implement a continuous data flow from a B channel to MICROWIRE interface, it is necessary to read register CR2 at each PCM frame.

II PROGRAMMABLE FUNCTIONS

For both formats of Digital Interface, programmable functions are configured by writing to a number of registers using a 2-byte write cycle.
Most of these registers can also be read-back for verification. Byte one is always register address, while byte two is Data.
Table 1 lists the register set and their respective adresses.

Table 1: Programmable Register Intructions

Function	Address byte								Data byte
	7	6	5	4	3	2	1	0	
Single byte Power up/down	P	X	X	X	X	X	0	X	none
Write CR0	P	0	0	0	0	0	1	X	see CR0 TABLE 2
Read-back CR0	P	0	0	0	0	1	1	X	see CR0
Write CR1	P	0	0	0	1	0	1	X	see CR1 TABLE 3
Read-back CR1	P	0	0	0	1	1	1	X	see CR1
Write Data to receive path	P	0	0	1	0	0	1	X	see CR2 TABLE 4
Read data from D_R	P	0	0	1	0	1	1	X	see CR2
Write Data to D_X	P	0	0	1	1	0	1	X	see CR3 TABLE 5
Write CR4	P	0	1	0	0	0	1	X	see CR4 TABLE 6
Read-back CR4	P	0	1	0	0	1	1	X	see CR4
Write CR5	P	0	1	0	1	0	1	X	see CR5 TABLE 7
Read-back CR5	P	0	1	0	1	1	1	X	see CR5
Write CR6	P	0	1	1	0	0	1	X	see CR6 TABLE 8
Read-back CR6	P	0	1	1	0	1	1	X	see CR6
Write CR7	P	0	1	1	1	0	1	X	see CR7 TABLE 9
Read-back CR7	P	0	1	1	1	1	1	X	see CR7
Write CR8	P	1	0	0	0	0	1	X	see CR8 TABLE 10
Read-back CR8	P	1	0	0	0	1	1	X	see CR8
Write CR9	P	1	0	0	1	0	1	X	see CR9 TABLE 11
Read-back CR9	P	1	0	0	1	1	1	X	see CR9
Write CR10	P	1	0	1	0	0	1	X	see CR10 TABLE 12
Read-back CR10	P	1	0	1	0	1	1	X	see CR10
Write CR11	P	1	0	1	1	0	1	X	see CR11 TABLE 13
Read-back CR11	P	1	0	1	1	1	1	X	see CR11
Write Test Register CR14	P	1	1	1	0	0	1	X	reserved

NOTE 1: bit 7 of the address byte and data byte is always the first bit clocked into or out from: CI and CO pins when MICROWIRE serial port is enabled.
X = reserved: write 0

NOTE 2: "P" bit is Power up/down Control bit. P = 1 Means Power Down.
Bit 1 indicates, if set, the presence of a second byte.

NOTE 3: Bit 2 is write/read select bit.

NOTE 4: Registers CR12, CR13, and CR15 are not accessible.

Table 2: Control Register CR0 Functions

7	6	5	4	3	2	1	0	Function	
F1	F0	CM	MA	IA	FF	B7	DL		
0	0							MCLK = 512 kHz *	
0	1							MCLK = 1.536 MHz	
1	0							MCLK = 2.048 MHz	
1	1							MCLK = 2.560 MHz	
		0						Linear code *	
		1						Companded code	
								Linear Code	Companded Code
			0	0				2-complement *	MU-law: CCITT D3-D4 *
			0	1				sign and magnitude	MU-law: Bare Coding
			1	0				2-complement	A-law including even bit inversion
			1	1				1-complement	A-law: Bare Coding
					0			B1 and B2 consecutive *	(1)
					1			B1 and B2 separated	(1)
						0		8 bits time-slot *	(1)
						1		7 bits time-slot	(1)
							0	Normal operation *	
							1	Digital Loop-back	

*: state at power on initialization

(1): significant in companded mode only

Table 3: Control Register CR1 Functions

7	6	5	4	3	2	1	0	Function	
DM1	DM0	DO	MR	MX	EN	TS			
0	X							delayed data timing *	
1	0							non-delayed normal data timing	
1	1							non-delayed reverse data timing	
		0						L0 latch set to 1 *	
		1						L0 latch set to 0	
			0					D_R connected to rec. path *	
			1					CR2 connected to rec. path	(1)
				0				Trans path connected to D_X *	
				1				CR3 connected to D_X	(1)
					0			voice data transfer disable *	
					1			voice data transfer enable	
						0		B1 channel selected *	(1)
						1		B2 channel selected	(1)
							X		

*: state at power on initialization

(1): significant in companded mode only

X: reserved: write 0

Table 4: Control Register CR2 Functions

7	6	5	4	3	2	1	0	Function
d7	d6	d5	d4	d3	d2	d1	d0	
msb							lsb	Data sent to Receive path or Data received from D_R input (1)

(1) Significant in companded mode only.

Table 5: Control Registers CR3 Functions

7	6	5	4	3	2	1	0	Function
d7	d6	d5	d4	d3	d2	d1	d0	
msb							lsb	D_X data transmitted (1)

(1) Significant in companded mode only

Table 6: Control Register CR4 Functions

7	6	5	4	3	2	1	0	Function
VS	TE	SI	OE1	OE2	RTE	HPB	SE	
0	0							Transmit input muted *
0	1							MIC1 Selected
1	0							MIC2 Selected
1	1							MIC3 Selected
		0						Internal sidetone disabled *
		1						Internal sidetone enabled
			0	0				Receive output muted *
			0	1				VFr output selected
			1	0				VLr output selected
			1	1				NOT ALLOWED
					0			Ring / Tone to V_{Fr} or V_{Lr} disabled *
					1			Ring / Tone to V_{Fr} or V_{Lr} enabled
						0		Receive HP filter enabled *
						1		Receive HP filter disabled
							0	Receive Signal to V_{Fr} or V_{Lr} disabled *
							1	Receive Signal to V_{Fr} or V_{Lr} enabled

*: state at power on initialization

X: reserved: write 0

Table 7: Control Register CR5 Functions

7	6	5	4	3	2	1	0	Function
Transmit amplifier				Sidetone amplifier				
0	0	0	0					0 dB gain *
0	0	0	1					1.5 dB gain
-	-	-	-					in 1.5 dB step
1	1	1	1					22.5 dB gain
				0	0	0	0	-12.5 dB gain *
				0	0	0	1	-13.5 dB gain
				-	-	-	-	in 1 dB step
				1	1	1	1	-27.5 dB gain

*: state at power on initialization

Table 8: Control Register CR6 Functions

7	6	5	4	3	2	1	0	Function
Earpiece ampifier [EARA]				Extra amplifier [EXTA]				
0	0	0	0					0 dB gain *
0	0	0	1					-2 dB gain
-	-	-	-					in 2 dB step
1	1	1	1					-30 dB gain
				0	0	0	0	0 dB gain *
				0	0	0	1	-2 dB gain
				-	-	-	-	in 2 dB step
				1	1	1	1	-30 dB gain

*: state at power on initialization

Table 9: Control Register CR7 Functions

7	6	5	4	3	2	1	0	Function		
Tone gain				F1	F2	SN	DE	Attenuation	f1 V_{pp}	f2 V_{pp}
0	0	0	0					0 dB *	1.6(2)	1.26(2)
0	0	0	1					-3 dB		
0	0	1	0					-6 dB		
0	0	1	1					- 9 dB		
0	1	0	0					-12 dB		
0	1	0	1					-15 dB		
0	1	1	0					-18 dB		
0	1	1	1					-21 dB		
1	X	X	0					-24 dB		
1	X	X	1					-27 dB	0.066	0.053
				0	0			f1 and f2 muted *		
				0	1			f2 selected		
				1	0			f1 selected		
				1	1			f1 and f2 in summed mode		
						0		Squarewave signal selected *		
						1		Sinewave signal selected		
							0	Normal operation *		
							1	Tone / Ring Generator connected to Transmit path		

*: state at power on initialization

(2): value provided if f1 or f2 is selected alone.
If f1 and f2 are selected in the summed mode, f1=0.89 V_{pp} while f2=0.7 V_{pp}.

X reserved: write 0

Table 10: Control Register CR8 Functions

7	6	5	4	3	2	1	0	Function
f17	f16	f15	f14	f13	f12	f11	f10	
msb							lsb	Binary equivalent of the decimal number used to calculate f1

Table 11: Control Register CR9 Functions

7	6	5	4	3	2	1	0	Function
f27	f26	f25	f24	f23	f22	f21	f20	
msb							lsb	Binary equivalent of the decimal number used to calculate f2

Table 12: Control Register CR10 Functions

7	6	5	4	3	2	1	0	Function
						DFT	HFT	
X	X	X	X	X	X			
						0	0	(*) Standard Frequency Tone Range
						0	1	Halved Frequency Tone Range
						1	0	Doubled Frequency Tone Range
						1	1	Forbidden

(*) Default values inserted into the Register at Power On.

X reserved, write 0.

Table 13: Control Register CR11 Functions

7	6	5	4	3	2	1	0	Function
BE	BI	BZ5	BZ4	BZ3	BZ2	BZ1	BZ0	
0								Buzzer output disabled (set to 0) *
1								Buzzer output enabled
	0							Duty Cycle is intended as the relative width of logic 1 *
	1							Duty cycle is intended as the relative width of logic 0
		msb					lsb	Binary equivalent of the decimal number used to calculate the duty cycle.

* state at power on initialization

CONTROL REGISTER CR0
First byte of a READ or a WRITE instruction to Control Register CR0 is as shown in TABLE 1. Second byte is as shown in TABLE 2.

Master Clock Frequency Selection
A master clock must be provided to ST5092 for operation of filter and coding/decoding functions.
MCLK frequency can be either 512 kHz, 1.536 MHz, 2.048 MHz or 2.56 MHz.
Bit F1 (7) and F0 (6) must be set during initialization to select the correct internal divider.
Default value is 512 kHz.
Any clock different from the default one must be selected prior a Power-Up instruction.

Coding Law Selection
Bits MA (4) and IA (3) permit selection of Mu-255 law or A law coding with or without even bit inversion if companded code (bit CM = 1) is selected.
Bits MA(4) and IA(3) permit selection of 2-complement, 1-complement or sign and magnitude if linear code (bit CM = 0) is selected.

Coding Selection
Bit CM (5) permits selection either of linear coding (14-bit) or companded coding (8-bit). Default value is linear coding.

Digital Interface format (1)
Bit FF(2) = 0 selects digital interface in Format 1 where B1 and B2 channel are consecutive. FF=1 selects Format 2 where B1 and B2 channel are separated by two bits. (See digital interface format section.)

56+8 selection (1)
Bit 'B7' (1) selects capability for ST5092 to take into account only the seven most significant bits of the PCM data byte selected.
When 'B7' is set, the LSB bit on D_R is ignored and LSB bit on Dx is high impedance. This function allows connection of an external "in band" data generator directly connected on the Digital Interface.

Digital loopback
Digital loopback mode is entered by setting DL bit(0) equal 1.
In Digital Loopback mode, data written into Receive PCM Data Register from the selected received time-slot is read-back from that Register in the selected transmit time-slot on Dx.
No PCM decoding or encoding takes place in this mode. Transmit and Receive amplifier stages are muted.

CONTROL REGISTER CR1
First byte of a READ or a WRITE instruction to Control Register CR1 is as shown in TABLE 1. Second byte is as shown in TABLE 3.

Digital Interface Timing
Bit DM1(7) = 0 selects digital interface in delayed timing mode, while DM1 = 1 and DM0 = 0 selects non-delayed normal data timing mode, and DM1 = 1 and DM0 = 1 selects non-delayed reverse data timing mode.
Default is delayed data timing.

Latch output control
Bit DO controls directly logical status of latch output LO: ie, a "ZERO" written in bit DO puts the output LO at logical 1, while a "ONE" written in bit DO sets the output LO to zero.

Microwire access to B channel on receive path (1)
Bit MR (4) selects access from MICROWIRE Register CR2 to Receive path. When bit MR is set high, data written to register CR2 is decoded each frame, sent to the receive path and data input at D_R is ignored.
In the other direction, current PCM data input received at D_R can be read from register CR2 each frame.

Microwire access to B channel on transmit path (1)
Bit MX (3) selects access from MICROWIRE write only Register CR3 to Dx output. When bit MX is set high, data written to CR3 is output at Dx every frame and the output of PCM encoder is ignored.

(1) Significant in companded mode only

	Mu 255 law								True A law even bit inversion								A law without even bit inversion							
	msb							lsb	msb							lsb	msb							lsb
Vin = + full scale	1	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0	1	1	1	1	1	1	1	1
Vin = 0 V	1	1	1	1	1	1	1	1	1	1	0	1	0	1	0	1	1	0	0	0	0	0	0	0
	0	1	1	1	1	1	1	1	0	1	0	1	0	1	0	1	1	0	0	0	0	0	0	0
Vin = - full scale	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	0	1	1	1	1	1	1	1

MSB is always the first PCM bit shifted in or out of: ST5092.

Transmit/Receive enabling/disabling
Bit 'EN' (2) enables or disables voice data transfer on D_X and D_R pins. When disabled, PCM data from DR is not decoded and PCM time-slots are high impedance on D_X. Default value is disabled.

B-channel selection (1)
Bit TS(1) permits selection between B1 or B2 channels. Default value is B1 channel.

CONTROL REGISTER CR2 (1)
Data sent to receive path or data received from D_R input. Refer to bit MR(4) in "Control Register CR1" paragraph.

CONTROL REGISTER CR3 (1)
D_X data transmitted. Refer to bit MX(3) in "Control Register CR1" paragraph.

CONTROL REGISTER CR4
First byte of a READ or a WRITE instruction to Control Register CR4 is as shown in TABLE 1. Second byte is as shown in TABLE 6.

Transmit Input Selection
MIC1 or MIC2 or MIC3 or transmit mute can be selected with bits 6 and 7 (V_S and TE).
Transmit gain can be adjusted within a 22.5 dB range in 1.5 dB step with Register CR5.

Sidetone Selection
Bit "SI" (5) enables or disables Sidetone circuitry. When enabled, sidetone gain can be adjusted with Register (CR5). When Transmit path is disabled, sidetone circuit is also disabled.

Output Driver Selection
Bits OE1(4) and OE2(3) provide the selection among the earpiece output or the extra amplifier output or both outputs muted.
OE1 = 1 and OE2 = 1 is not allowed.

Ring/Tone signal selection
Bit RTE (2) provide select capability to connect on-chip Ring/Tone generator either to an extra amplifier input or to earpiece amplifier input.

Receive High Pass Filter Selection
Bit HPB (1) provide the selection of the receive high pass filter cutoff frequency.

PCM receive data selection
Bits "SE" (0) provide select capability to connect received speech signal either to an extra amplifier input or to earpiece amplifier input.

CONTROL REGISTER CR5
First byte of a READ or a WRITE instuction to Control Register CR5 is as shown in TABLE 1. Second byte is as shown in TABLE 7.

Transmit gain selection
Transmit amplifier can be programmed for a gain from 0dB to 22.5dB in 1.5dB step with bits 4 to 7.
0 dBmO level at the output of the transmit amplifier (A reference point) is 0.492 Vrms (overload voltage is 0.707 Vrms).

Sidetone attenuation selection
Transmit signal picked up after the switched capacitor low pass filter may be fed back into both Receive amplifiers.
Attenuation of the signal at the output of the sidetone attenuator can be programmed from –12.5dB to -27.5dB relative to reference point A in 1 dB step with bits 0 to 3.

CONTROL REGISTER CR6
First byte of a READ or a WRITE instruction to Control Register CR6 is as shown in TABLE 1. Second byte is as shown in TABLE 8.

Earpiece amplifier gain selection:
Earpiece Receive gain can be programmed in 2 dB step from 0 dB to -30 dB relative to the maximum with bits 4 to 7.
0 dBmO voltage at the output of the amplifier on pins V_{Fr+} and V_{Fr-} is then 1.965 Vrms when 0dB gain is selected down to 61.85 Vrms when -30dB gain is selected.

Extra amplifier gain selection:
Extra Receive amplifier gain can be programmed in 2 dB step from 0 dB to -30 dB relative to the maximum with bits 0 to 3.
0 dBmO voltage on the output of the amplifier on pins V_{Lr+} and V_{Lr-} 1.965 Vrms when 0 dB gain is selected down to 61.85 mVrms when -30 dB gain is selected.

CONTROL REGISTER CR7:
First byte of a READ or a WRITE instruction to Control Register CR7 is as shown in TABLE 1. Second byte is as shown in TABLE 9.

(1) Significant in companded mode only

Tone/Ring amplifier gain selection
Output level of Ring/Tone generator, before attenuation by programmable attenuator is 1.6 Vpk-pk when f1 generator is selected alone or summed with the f2 generator and 1.26 Vpk-pk when f2 generator is selected alone.
Selected output level can be attenuated down to -27 dB by programmable attenutator by setting bits 4 to 7.

Frequency mode selection
Bits 'F1' (3) and 'F2' (2) permit selection of f1 and/or f2 frequency generator according to TABLE 9.
When f1 (or f2) is selected, output of the Ring/Tone is a squarewave (or a sinewave) signal at the frequency selected in the CR8 (or CR9) Register.
When f1 and f2 are selected in summed mode, output of the Ring/Tone generator is a signal where f1 and f2 frequency are summed.
In order to meet DTMF specifications, f2 output level is attenuated by 2dB relative to the f1 output level.
Frequency temporization must be controlled by the microcontroller.

Waveform selection
Bit 'SN' (1) selects waveform of the output of the Ring/Tone generator. Sinewave or squarewave signal can be selected.

DTMF selection
Bit DE (0) permits connection of Ring/Tone/DTMF generator on the Transmit Data path instead of the Transmit Amplifier output. Earpiece or extra receive output feed-back may be provided by sidetone circuitry by setting bit SI or directly by setting bit RTE in Register CR4. Loudspeaker feed-back may be provided directly by setting bit RTL in Register CR4.

CONTROL REGISTERS CR8 AND CR9
First byte of a READ or a WRITE instruction to Control Register CR8 or CR9 is as shown in TABLE 1. Second byte is respectively as shown in TABLE 10 and 11.
If "standard frequency tone range" is selected, Tone or Ring signal frequency value is defined by the formula:

f1 = CR8 / 0.128 Hz

and

f2 = CR9 / 0.128 Hz

where CR8 and CR9 are decimal equivalents of the binary values of the CR8 and CR9 registers respectively. Thus, any frequency between 7.8 Hz and 1992 Hz may be selected in 7.8 Hz step.
If "halved frequency tone range"is selected, Tone or Ring signal frequency value is defined by the formula:

f1 = CR8 / 0.256 Hz

and

f2 = CR9 / 0.256 Hz

This any frequency between 3.9Hz and 996Hz may be selected in 3.9Hz step.
If "doubled frequency tone range"is selected, Tone or Ring signal frequency value is defined by the formula:

f1 = CR8 / 0.064 Hz

and

f2 = CR9 / 0.064 Hz

Thus any frequency between 15.6Hz and 3984Hz may be selected in 15.6Hz step.

TABLE 12 gives examples for the main frequencies usual for Tone or Ring generation.

CONTROL REGISTER CR10
Bit DFT(1) and HFT(0) permits the selection among "standard frequency tone range" (i.e. from 7.8Hz to 1992Hz in 7.8Hz step), "halved frequency tone range" (i.e. from 3.9Hz to 996Hz in 3.9Hz step), and "doubled frequency tone range" (i.e. from 15.6Hz to 3984Hz in 15.6Hz step) according to the values described in CONTROL REGISTER CR8 and CR9.

CONTROL REGISTER CR11
Bit BE(7) permits connection of a f1 squarewave PWM Ring signal, amplitude modulated or not by a f2 squarewave signal, to buzzer driver output BZ. Bits BZ5 to BZ0 define the duty cycle of the PWM squarewave, according to the following formula:

$$\text{Duty Cycle} = CR11(5 \div 0) \times 0.78125\%$$

where CR11(5 ÷ 0) is the decimal equivalent of the binary value BZ5 ÷ BZ0.

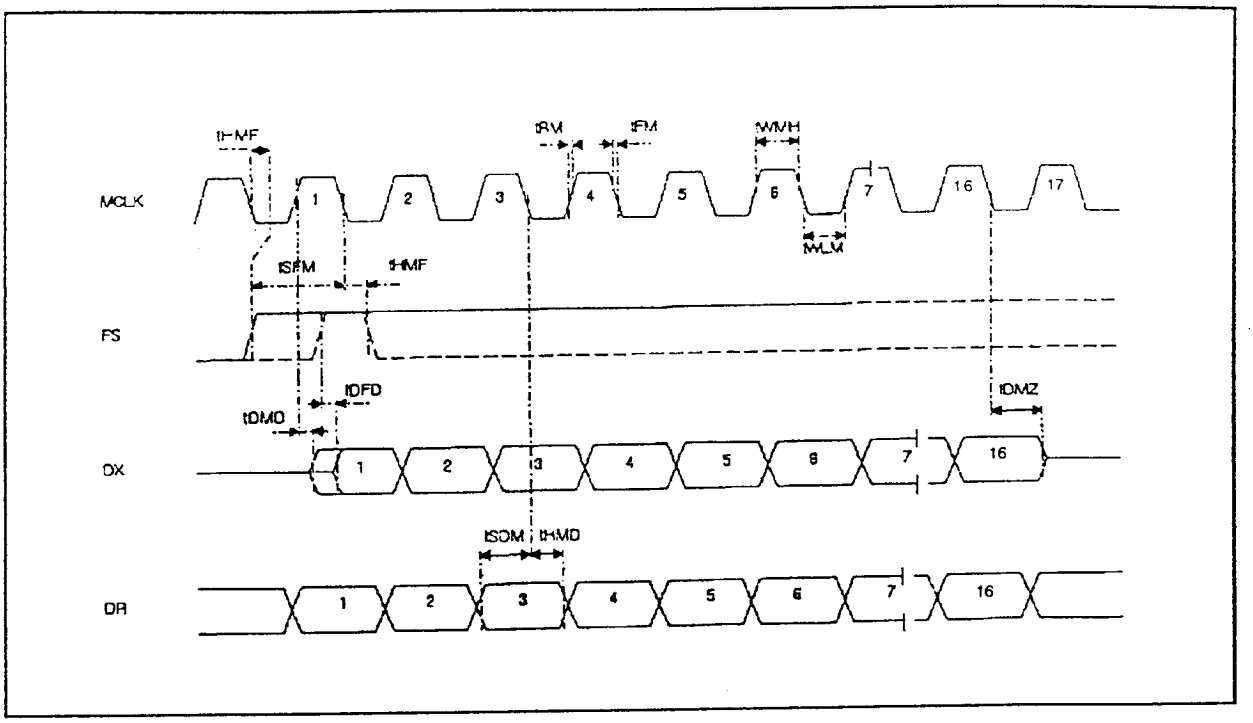
When BE = 1, if bits F1 = 1 and F2 = 0 in register CR7, a f1 PWM ring signal is present at the buzzer output, while if bits F1 = 1 and F2 = 1 in register CR7 the f1 PWM ring signal is also amplitude modulated by a f2 squarewave frequency. Bit BI (6) allows to chose the logic level at which the duty cycle is referred: BI = 0 means that duty cycle is intended as the relative width of the logic1, while BI = 1 means that duty cycle is intended as the relative width of the logic 0. When BE = 0 (or during power down) BZ = 0 if BI = 0 or BZ = 1 if BI = 1.

Table 12: Examples of Usual Frequency Selection (Standard frequency tone range)

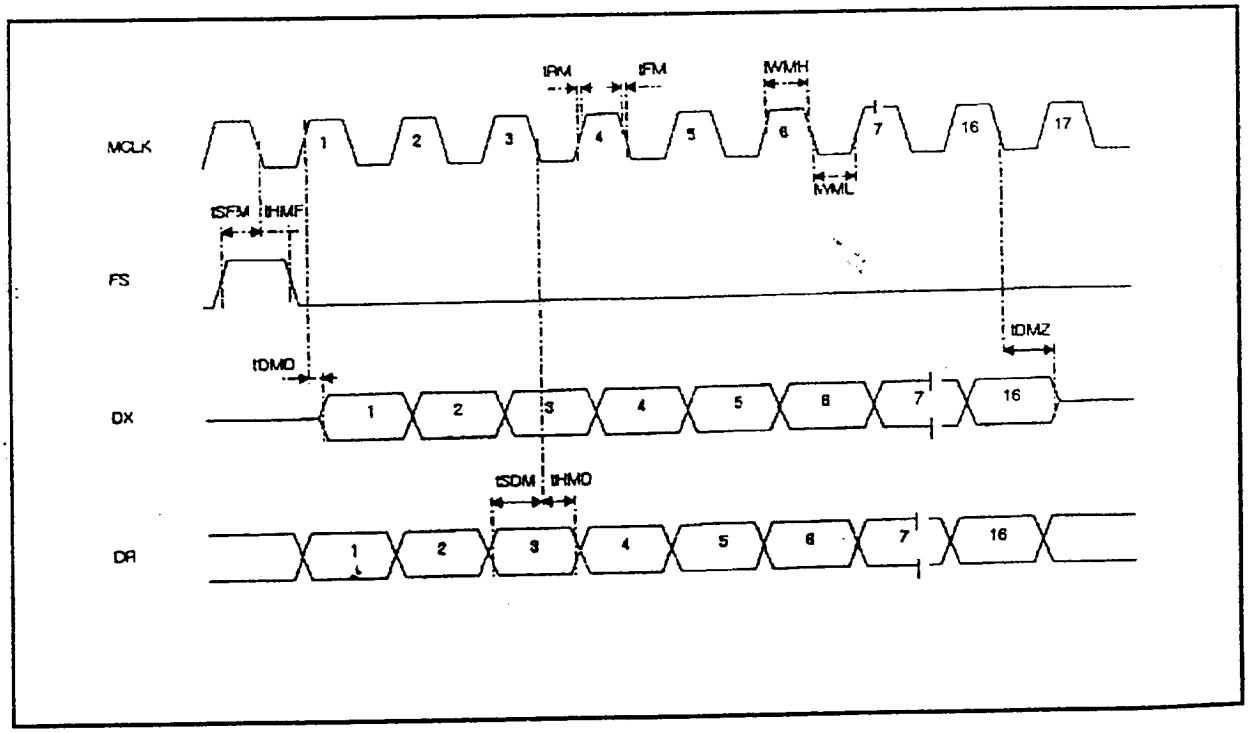
Description	f1 value (decimal)	Theoretic value (Hz)	Typical value (Hz)	Error %
Tone 250 Hz	32	250	250	.00
Tone 330 Hz	42	330	328.2	-.56
Tone 425 Hz	54	425	421.9	-.73
Tone 440 Hz	56	440	437.5	-.56
Tone 800 Hz	102	800	796.9	-.39
Tone 1330 Hz	170	1330	1328.1	-.14
DTMF 697 Hz	89	697	695.3	-.24
DTMF 770 Hz	99	770	773.4	+.44
DTMF 852 Hz	109	852	851.6	-.05
DTMF 941 Hz	120	941	937.5	-.37
DTMF 1209 Hz	155	1209	1210.9	+.16
DTMF 1336 Hz	171	1336	1335.9	-.01
DTMF 1477 Hz	189	1477	1476.6	.00
DTMF 1633 Hz	209	1633	1632.8	.00
SOL	50	392	390.6	-.30
LA	56	440	437.5	-.56
SI	63	494	492.2	-.34
DO	67	523.25	523.5	+.04
RE	75	587.33	586.0	-.23
MI flat	80	622.25	625.0	+.45
MI	84	659.25	656.3	-.45
FA	89	698.5	695.3	-.45
FA sharp	95	740	742.2	+.30
SOL	100	784	781.3	-.34
SOL sharp	106	830.6	828.2	-.29
LA	113	880	882.9	+.33
SI	126	987.8	984.4	-.34
DO	134	1046.5	1046.9	+.04
RE	150	1174.66	1171.9	-.23
MI	169	1318.5	1320.4	+.14

TIMING DIAGRAM

Non Delayed Data Timing Mode (Normal) (*)



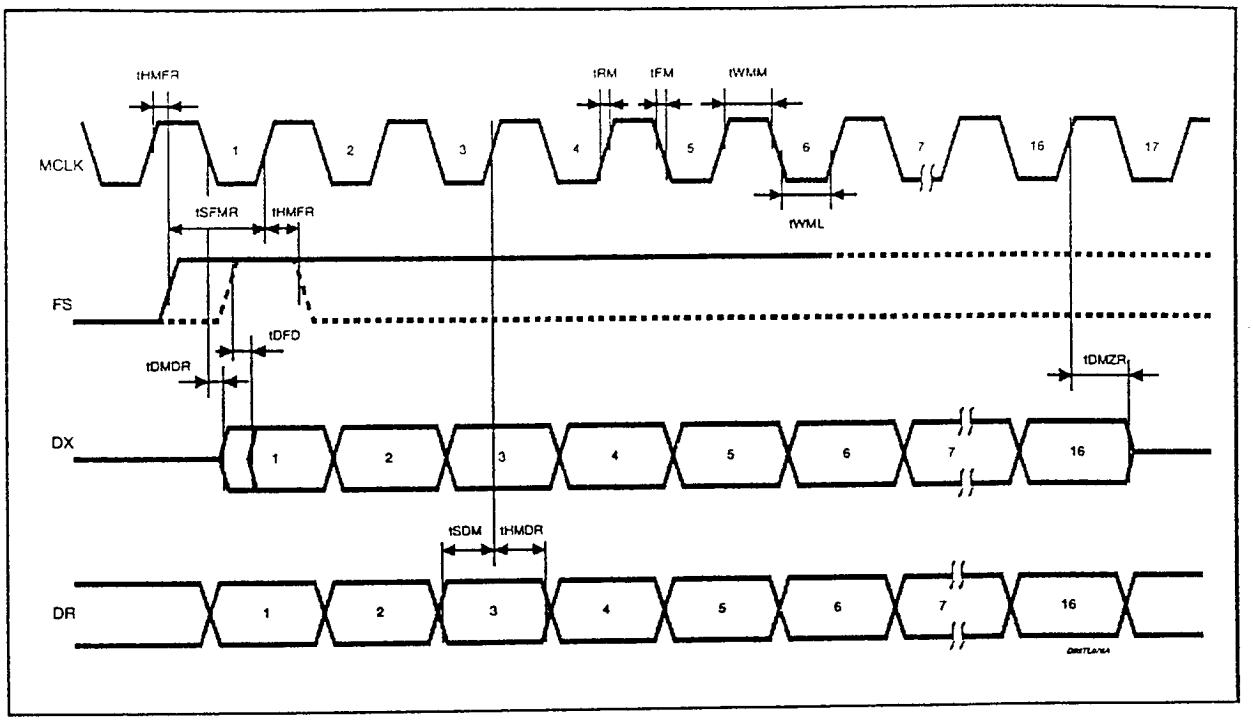
Delayed Data Timing Mode (*)



(*) In the case of companded code the timing is applied to 8 bits instead of 16 bits (see ST5080A data sheet)

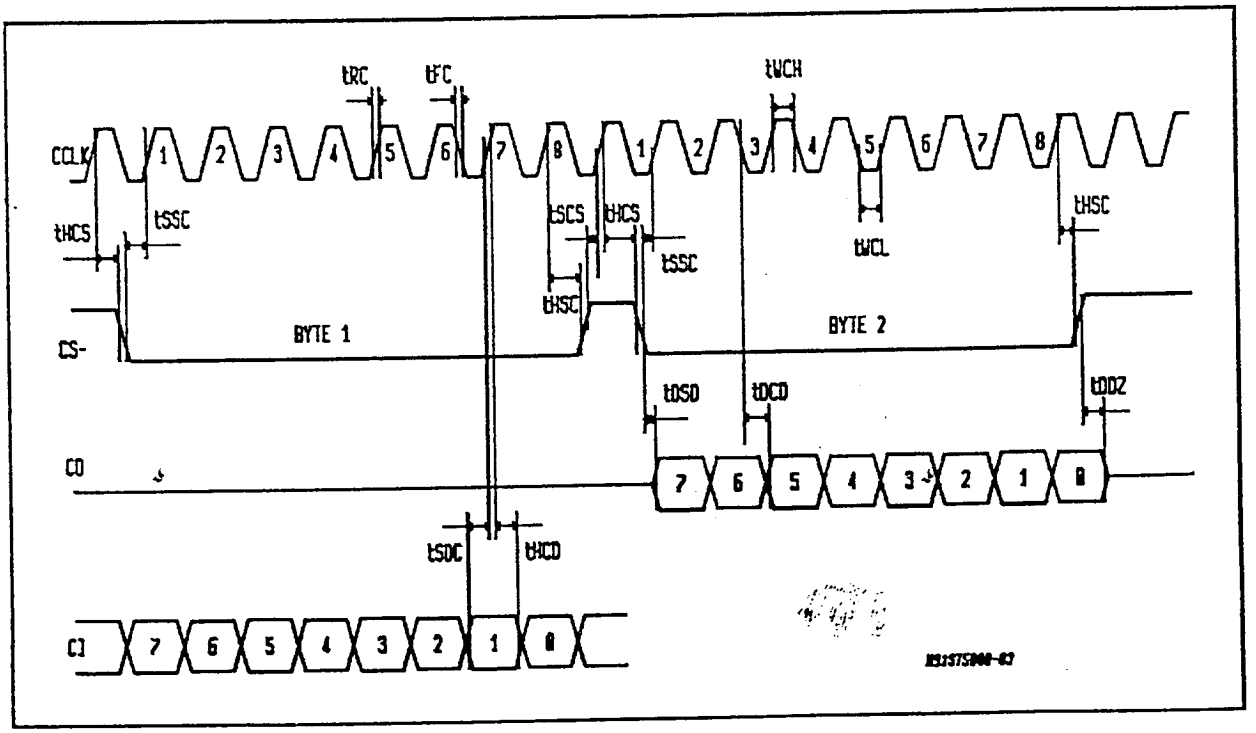
TIMING DIAGRAM (continued)

Non Delayed Reverse Data Timing Mode (*)



(*) In the case of companded code the timing is applied to 8 bits instead of 16 bits.

Serial Control Timing (MICROWIRE MODE)



ABSOLUTE MAXIMUM RATINGS

Parameter	Value	Unit
V_{CC} to GND	5.5	V
Voltage at MIC ($V_{CC} \leq 3.6V$)	V_{CC} +1 to GND -1	V
Current at V_{Fr} and V_{Lr}	$\pm$ 100	mA
Current at any digital output	$\pm$ 50	mA
Voltage at any digital input ($V_{CC} \leq 3.6V$); limited at $\pm$ 50mA	V_{CC} + 1 to GND - 1	V
Storage temperature range	- 65 to + 150	°C
Lead Temperature (wave soldering, 10s)	+ 260	°C

TIMING SPECIFICATIONS (unless otherwise specified, V_{CC} = 2.7V to 3.6V, T_A = –30°C to 85°C ; typical characteristics are specified V_{CC} = 3.0V, T_A = 25 °C; all signals are referenced to GND, see Note 5 for timing definitions)

NOTICE: All timing specifications can be changed.

MASTER CLOCK TIMING

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
f_{MCLK}	Frequency of MCLK	Selection of frequency is programmable (see table 2)		512 1.536 2.048 2.560		kHz MHz MHz MHz
t_{WMH}	Period of MCLK high	Measured from V_{IH} to V_{IH}	80			ns
t_{WML}	Period of MCLK low	Measured from V_{IL} to V_{IL}	80			ns
t_{RM}	Rise Time of MCLK	Measured from V_{IL} to V_{IH}			30	ns
t_{FM}	Fall Time of MCLK	Measured from V_{IH} to V_{IL}			30	ns

PCM INTERFACE TIMING

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
t_{HMF}	Hold Time MCLK low to FS low		0			ns
t_{SFM}	Setup Time, FS high to MCLK low		30			ns
t_{DMD}	Delay Time, MCLK high to data valid	Load = 100 pf			100	ns
t_{DMZ}	Delay Time, MCLK low to DX disabled		10		100	ns
t_{DFD}	Delay Time, FS high to data valid	Load = 100 pf ; Applies only if FS rises later than MCLK rising edge in Non Delayed Mode only			100	ns
t_{SDM}	Setup Time, D_R valid to MCLK receive edge		20			ns
t_{HMD}	Hold Time, MCLK low to D_R invalid		10			ns
t_{HMFR}	Hold Time MCLK High to FS low		30			ns
t_{SFMR}	Setup Time, FS high to MCLK High		30			ns
t_{DMDR}	Delay Time, MCLK low to data valid	Load = 100pF			100	ns
t_{DMZR}	Delay Time, MCLK High to DX disabled		10		100	ns
t_{HMDR}	Hold Time, MCLK High to D_R invalid		20			ns

SERIAL CONTROL PORT TIMING

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
f_{CCLK}	Frequency of CCLK				2.048	MHz
t_{WCH}	Period of CCLK high	Measured from V_{IH} to V_{IH}	160			ns
t_{WCL}	Period of CCLK low	Measured from V_{IL} to V_{IL}	160			ns
t_{RC}	Rise Time of CCLK	Measured from V_{IL} to V_{IH}			50	ns
t_{FC}	Fall Time of CCLK	Measured from V_{IH} to V_{IL}			50	ns
t_{HCS}	Hold Time, CCLK high to CS– low		10			ns
t_{SSC}	Setup Time, CS–low to CCLK high		50			ns
t_{SDC}	Setup Time, CI valid to CCLK high		50			ns
t_{HCD}	Hold Time, CCLK high to CI invalid		50			ns
t_{DCD}	Delay Time, CCLK low to CO data valid	Load = 100 pF			80	ns
t_{DSD}	Delay Time, CS–low to CO data valid				50	ns
t_{DDZ}	Delay Time CS–high or 8th CCLK low to CO high impedance whichever comes first		10		80	ns
t_{HSC}	Hold Time, 8th CCLK high to CS– high		100			ns
t_{SCS}	Setup Time, CS–high to CCLK high		100			ns

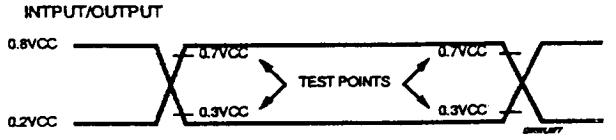
Note 5: A signal is valid if it is above V_{IH} or below V_{IL} and invalid if it is between V_{IL} and V_{IH}.
For the purpoes of this specification the following conditions apply:
a) All input signal are defined as: $V_{IL} = 0.2V_{CC}$, $V_{IH} = 0.8V_{CC}$, $t_R < 10ns$, $t_F < 10ns$.
b) Delay times are measured from the inputs signal valid to the output signal valid.
c) Setup times are measured from the data input valid to the clock input invalid.
d) Hold times are measured from the clock signal valid to the data input invalid.

ELECTRICAL CHARACTERISTICS (unless otherwise specified, V_{CC} = 2.7V to 3.6V, T_A = –30°C to 85°C ; typical characteristic are specified at V_{CC} = 3.0V, T_A = 25°C ; all signals are referenced to GND)

DIGITAL INTERFACES

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
V_{IL}	Input Low Voltage	All digital inputs	DC			$0.3V_{CC}$	V
			AC			$0.2V_{CC}$	V
V_{IH}	Input High Voltage	All digital inputs	DC	$0.7V_{CC}$			V
			AC	$0.8V_{CC}$			V
V_{OL}	Output Low Voltage	All digital outputs, $I_L = 10\mu A$ All digital outputs, $I_L = 2mA$				0.1 0.4	V V
V_{OH}	Output High Voltage	All digital outputs, $I_L = 10\mu A$ All digital outputs, $I_L = 2mA$		V_{CC}-0.1 V_{CC}-0.4			V V
I_{IL}	Input Low Current	Any digital input, $GND < V_{IN} < V_{IL}$		-10		10	µA
I_{IH}	Input High Current	Any digital input, $V_{IH} < V_{IN} < V_{CC}$		-10		10	µA
I_{OZ}	Output Current in High impedance (Tri-state)	D_X and CO		-10		10	µA

A.C. TESTING INPUT, OUTPUT WAVEFORM



AC Testing: inputs are driven at $0.8V_{CC}$ for a logic "1"and 0.2VCC for a logic "0 ". Timing measurements are made at $0.7V_{CC}$ for a logic "1"and $0.3V_{CC}$ for a logic "0".

ANALOG INTERFACES

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
I_{MIC}	Input Leakage	GND < V_{MIC} < V_{CC}	-100		+100	µA
R_{MIC}	Input Resistance	GND < V_{MIC} < V_{CC}	50			kΩ
R_{LVFr}	Load Resistance (*)	V_{Fr+} to V_{Fr-}	30			Ω
C_{LVFr}	Load Capacitance (*)	From V_{Fr+} to V_{Fr-}		50		nF
R_{OVFr0}	Output Resistance	Steady zero PCM code applied to DR; I = ± 1mA		1.0		Ω
V_{OSVFr0}	Differential offset: Voltage at V_{Fr+}, V_{Fr-}	Alternating ± zero PCM code applied to DR maximum receive gain; R_L = 100Ω	-100		+100	mV
R_{LvLr}	Load Resistance (*)	V_{Lr+} to V_{Lr-}	30			Ω
C_{LvLr}	Load Capacitance (*)	from V_{Lr+} to V_{Lr-}		50		nF
R_{OLVr0}	Output Resistance	Steady zero PCM code applied to DR; I ± 1mA		1		Ω
V_{OSVLr0}	Differential offset Voltage at V_{Lr+}, V_{Lr-}	Alternating ± zero PCM code applied to DR maximum receive gain; R_L = 50Ω	−100		+100	mV

(*) See application note for V_{Fr} and V_{Lr} connections.

POWER DISSIPATION

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
I_{CC0}	Power down Current	CCLK,CI = 0.1V; CS = V_{CC}-0.1V		0.5	5	µA
I_{CC1}	Power Up Current	V_{Lr+}, V_{Lr-} and V_{Fr+}, V_{Fr-} not loaded		5	8	mA

TRANSMISSION CHARACTERISTICS (unless otherwise specified, V_{CC} = 2.7V to 3.6V, T_A = −30°C to 85°C; typical characteristics are specified at V_{CC} = 3.0V, T_A = 25°C, MIC1/2/3 = 0dBm0, D_R = −6dBm0 PCM code, f = 1015.625 Hz; all signal are referenced to GND)

AMPLITUDE RESPONSE (Maximum, Nominal, and Minimum Levels)
Transmit path - Absolute levels at MIC1 / MIC2 / MIC3

Parameter	Test Condition	Min.	Typ.	Max.	Unit
0 dBm0 level	Transmit Amps connected for 20dB gain		49.26		mV_{RMS}
Overload level			70.71		mV_{RMS}
0 dBm0 level	Transmit Amps connected for 42.5dB gain		3.694		mV_{RMS}
Overload level			5.302		mV_{RMS}

TRANSMISSION CHARACTERISTICS (continued)

AMPLITUDE RESPONSE (Maximum, Nominal, and Minimum Levels)
Receive path - Absolute levels at V_{FR} (Differentially measured)

Parameter	Test Condition	Min.	Typ.	Max.	Unit
0 dBM0 level	Receive Amp programmed for 0dB gain		1.965		V_{RMS}
0 dBM0 level	Receive Amp programmed for - 30dB attenuation		61.85		mV_{RMS}

AMPLITUDE RESPONSE (Maximum, Nominal, and Minimum Levels)
Receive path - Absolute levels at V_{Lr} (Differentially measured)

Parameter	Test Condition	Min.	Typ.	Max.	Unit
0 dBM0 level	Receive Amp programmed for 0dB gain		1.965		V_{RMS}
0 dBM0 level	Receive Amp programmed for - 30dB gain		61.85		mV_{RMS}

AMPLITUDE RESPONSE
Transmit path

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
G_{XA}	Transmit Gain Absolute Accuracy	Transmit Gain Programmed for minimum. Measure deviation of Digital PCM Code from ideal $0dB_{m0}$ PCM code at D_X	-0.5		0.5	dB
G_{XAG}	Transmit Gain Variation with programmed gain	Measure Transmit Gain over the range from Maximum to minimum setting. Calculate the deviation from the programmed gain relative to GXA, i.e. $G_{AXG} = G_{actual} - G_{prog.} - G_{XA}$	-0.5		0.5	dB
G_{XAT}	Transmit Gain Variation with temperature	Measured relative to G_{XA}. min. gain < G_X < Max. gain	-0.1		0.1	dB
G_{XAV}	Transmit Gain Variation with supply	Measured relative to G_{XA} G_X = Minimum gain	-0.1		0.1	dB
G_{XAF}	Transmit Gain Variation with frequency	Relative to 1015,625 Hz, multitone test technique used. min. gain < G_X < Max. gain f = 60 Hz f = 100 Hz f = 200 Hz f = 300 Hz f = 400 Hz to 3000 Hz f = 3400 Hz f = 4000 Hz f = 4600 Hz (*) f = 8000 Hz (*)	 -1.5 -0.5 -1.5		 -30 -20 -6 0.5 0.5 0.0 -14 -35 -47	 dB dB dB dB dB dB dB dB dB
G_{XAL}	Transmit Gain Variation with signal level	Sinusoidal Test method. Reference Level = -10 dBm0 V_{MIC} = -40 dBm0 to +3 dBm0 V_{MIC} = -50 dBm0 to -40 dBm0 V_{MIC} = -55 dBm0 to -50 dBm0	 -0.5 -0.5 -1.2		 0.5 0.5 1.2	 dB dB dB

(*) The limit at frequencies between 4600Hz and 8000Hz lies on a straight line connecting the two frequencies on a linear (dB) scale versus log (Hz) scale.

AMPLITUDE RESPONSE
Receive path

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
G_{RAE}	Receive Gain Absolute Accuracy	Receive gain programmed for maximum Apply -6 dB_{m0} PCM code to D_R Measure V_{Fr}	-0.5		0.5	dB
G_{RAL}	Receive Gain Absolute Accuracy	Receive gain programmed for maximum Apply -6 dB_{m0} PCM code to D_R Measure V_{Lr}	-0.5		0.5	dB
G_{RAGE}	Receive Gain Variation with programmed gain	Measure V_{Fr} Gain over the range from Maximum to minimum setting. Calculate the deviation from the programmed gain relative to GRAE, i.e. $G_{RAGE} = G_{actual} - G_{prog.} - G_{RAE}$	-0.5		0.5	dB
G_{RAGL}	Receive Gain Variation with programmed gain	Measure V_{Lr} Gain over the range from Maximum to minimum setting. Calculate the deviation from the programmed gain relative to GRAL, i.e. $G_{RAGL} = G_{actual} - G_{prog.} - G_{RAL}$	-0.5		0.5	dB
G_{RAT}	Receive Gain Variation with temperature	Measured relative to GRA. (V_{Lr} and V_{Fr}) min. gain < GR < Max. gain	-0.1		0.1	dB
G_{RAV}	Receive Gain Variation with Supply	Measured relative to GRA. (V_{Lr} and V_{Fr}) G_R = Maximum Gain	-0.1		0.1	dB
G_{RAF}	Receive Gain Variation with frequency (V_{Lr} and V_{Fr}) HPB = 0	Relative to 1015,625 Hz, multitone test technique used. min. gain < G_R < Max. gain f = 60Hz f = 100Hz f = 200 Hz f = 300 Hz f = 400 Hz to 3000 Hz f = 3400 Hz f = 4000 Hz	 -1.5 -0.5 -1.5		 -20 -12 -2 0.5 0.5 0.0 -14	 dB dB dB dB dB dB dB
	Receive Gain Variation with frequency (V_{Lr} and V_{Fr}) HPB = 1	Relative to 1015,625 Hz, multitone test technique used. min. gain < G_R < Max. gain f = 50Hz f = 100 Hz to 3000 Hz f = 3400 Hz f = 4000 Hz	 -1.5 -0.5 -1.5		 0.5 0.5 0.0 -14	 dB dB dB dB
$G_{RAL\,E}$	Receive Gain Variation with signal level (V_{Fr})	Sinusoidal Test Method Reference Level = –10 dBm0 D_R = -40 dBm0 to -3 dBm0 D_R = -50 dBm0 to -40 dBm0 D_R = -55 dBm0 to -50 dBm0	 -0.5 -0.5 -1.2		 0.5 0.5 1.2	 dB dB dB
$G_{RAL\,L}$	Receive Gain Variation with signal level (V_{Lr})	Sinusoidal Test Method Reference Level = –10 dBm0 D_R = -40 dBm0 to -3 dBm0 D_R = -50 dBm0 to -40 dBm0 D_R = -55 dBm0 to -50 dBm0	 -0.5 -0,5 -1.2		 0.5 0.5 1.2	 dB dB dB

ENVELOPE DELAY DISTORTION WITH FREQUENCY

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
DXA	Tx Delay, Absolute	f = 1600 Hz		320		µs
DXR	Tx Delay, Relative	f = 500 - 600 Hz f = 600 - 800 Hz f = 800 - 1000 Hz f = 1000 - 1600 Hz f = 1600 - 2600 Hz f = 2600 - 2800 Hz f = 2800 - 3000 Hz		290 180 50 20 55 80 180		µs µs µs µs µs µs µs
DRA	Rx Delay, Absolute	f = 1600 Hz		280		µs
DRR	Rx Delay, Relative	f = 500 - 600 Hz f = 600 - 800 Hz f = 800 - 1000 Hz f = 1000 - 1600 Hz f = 1600 - 2600 Hz f = 2600 - 2800 Hz f = 2800 - 3000 Hz		200 110 50 20 65 100 220		µs µs µs µs µs µs µs

NOISE

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
NXP	Tx Noise, P weighted (up to 35dB)	V_{MIC} = 0V, DE = 0		-75	-70	dBm0p
NRP	Rx Noise, A weighted (max. gain)	Receive PCM code = Positive Zero SI = 0 and RTE = 0		120	150	µVrms (*)
NRS	Noise, Single Frequency	MIC = 0V, Loop-around measurament from f = 0 Hz to 100 kHz		-50		dBm0
PPSRx	PSRR, Tx	MIC = 0V, V_{CC} = 3.3 V_{DC} + 50 mV_{rms}; f = 0Hz to 50KHz	30	60		dB
PPSRp	PSRR, Rx	PCM Code equals Positive Zero, V_{CC} = 3.3 VDC + 50 mVrms, f = 0 Hz - 4 kHz f = 4 kHz - 50 kHz	 30 30	 70 70		 dB dB
SOS	Spurious Out-Band signal at the output	DR input set to -6 dBm0 PCM code 300 - 3400 Hz Input PCM Code applied at DR 4600 Hz - 5600 Hz 5600 Hz - 7600 Hz 7600 Hz - 8400 Hz			 -40 -50 -50	 dB dB dB

(*) A Weighted

DISTORTION

Symbol	Parameter	Test Condition	Min.	Min. (#)	Typ.	Max.	Unit
S_{TDX} (*)	Signal to Total Distortion (up to 35dB gain)	Sinusoidal Test Method (measured using linear 300 to 3400 weighting)					
	Typical values are measured with 30.5dB gain	Level = 0 dBm0	56	56	65		dB
		Level = -6 dBm0	50	50	64		dB
		Level = -10 dBm0	48	48	61		dB
		Level = -20 dBm0	43	43	52		dB
		Level = -30 dBm0	38	37.5	42		dB
		Level = -40 dBm0	29	28.5	31		dB
		Level = -45 dBm0	24	23	26		dB
		Level = -55 dBm0	15	13	16		dB
S_{DFx}	Single Frequency Distortion transmit	0 dBm0 input signal			-80	-56	dB
S_{TDRE} (*)	Signal to Total Distortion (VFr) (up to 20dB attenuation)	Sinusoidal Test Method (measured using linear 300 to 3400 weighting)					
	Typical values are measured with 20dB attenuation.	Level = -6 dBm0	50		64		dB
		Level = -10 dBm0	48		62		dB
		Level = -20 dBm0	43		53		dB
		Level = -30 dBm0	38		43		dB
		Level = -40 dBm0	29		33		dB
		Level = -45 dBm0	24		28		dB
		Level = -55 dBm0	15		18		dB
S_{DFr}	Single Frequency Distortion receive (V_{Fr})	-6 dBm0 input signal			-80	-50	dB
S_{TDRL} (*)	Signal to Total Distortion (VLr) (up to 20dB attenuation)	Sinusoidal Test Method (measured using linear 300 to 3400 weighting)					
	Typical values are measured with 20dB attenuation	Level = -6 dBm0	50		64		dB
		Level = -10 dBm0	48		62		dB
		Level = -20 dBm0	43		53		dB
		Level = -30 dBm0	38		43		dB
		Level = -40 dBm0	29		33		dB
		Level = -45 dBm0	24		28		dB
		Level = -55 dBm0	15		18		dB
S_{DLr}	Single Frequency Distortion receive (V_{Lr})	-6 dBm0 input signal			-80	-50	dB
IMD	Intermodulation	Loop-around measurement Voltage at MIC = -10 dBm0 to -27 dBm0, 2 Frequencies in the range 300 - 3400 Hz			-75	-46	dB

(*) The limit curve shall be determined by straight lines joining successive coordinates given in the table.

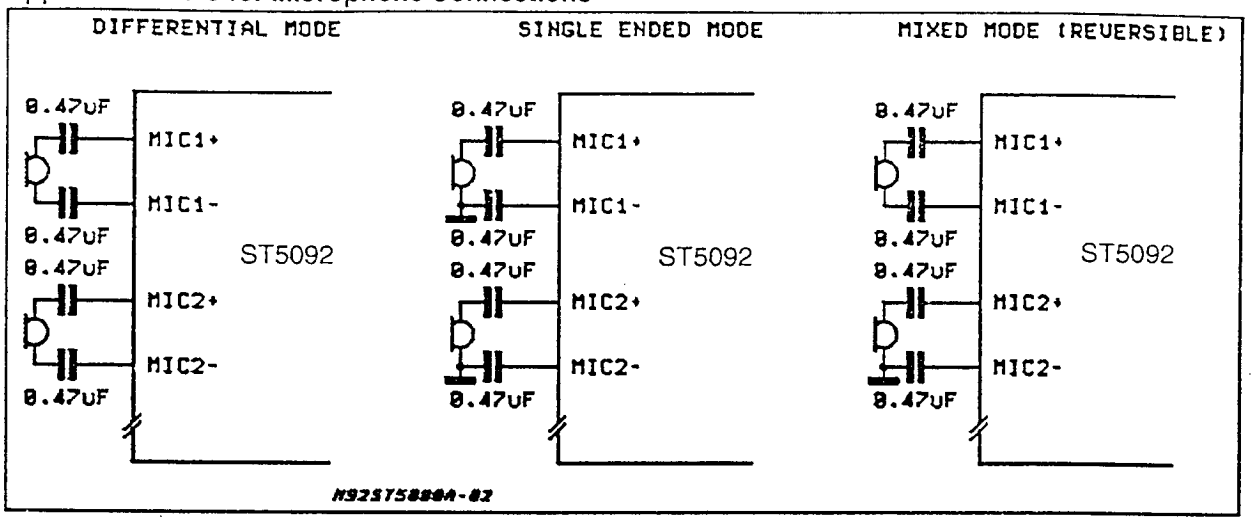
(#) Lower limits used during the automatic testing to avoid unrealistic yield loss due to ±2dB imprecision of time-limited noise measurements.

CROSSTALK

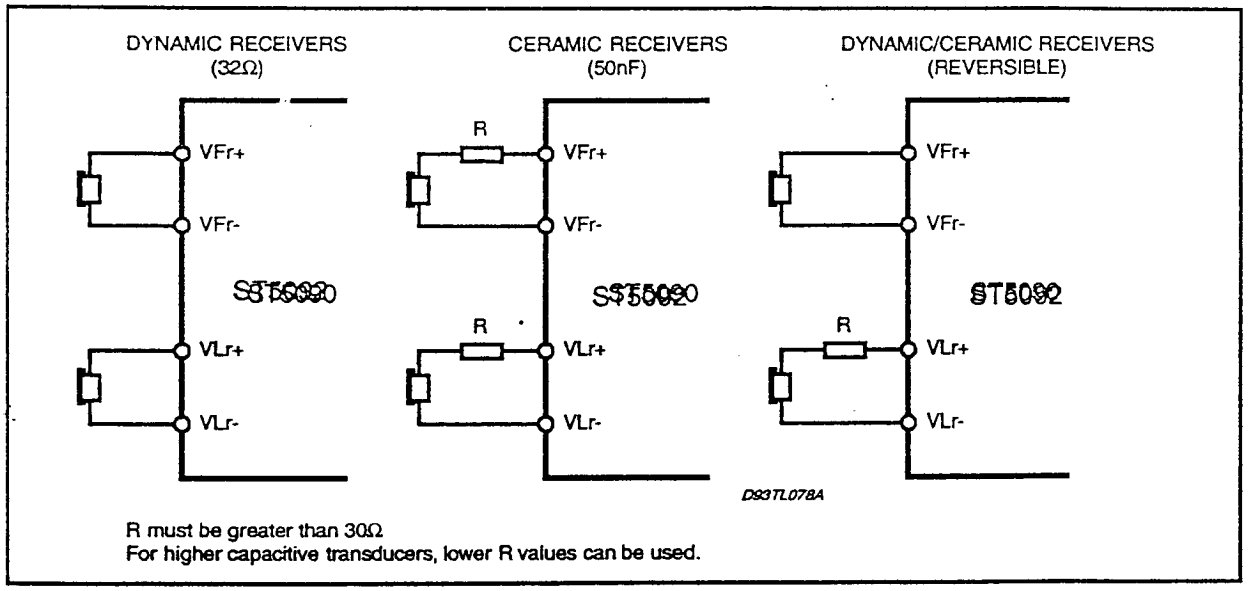
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
C_{Tx-r}	Transmit to Receive	Transmit Level = 0 dBm0, f = 300 - 3400 Hz DR = Quiet PCM Code		-100	-65	dB
C_{Tr-x}	Receive to Transmit	Receive Level = -6 dBm0, f = 300 - 3400 Hz MIC = 0V		-80	-65	dB

APPLICATIONS

Application Note for Microphone Connections



Application Note for V_{Fr} and V_{Lr} Connections



R must be greater than 30Ω
For higher capacitive transducers, lower R values can be used.

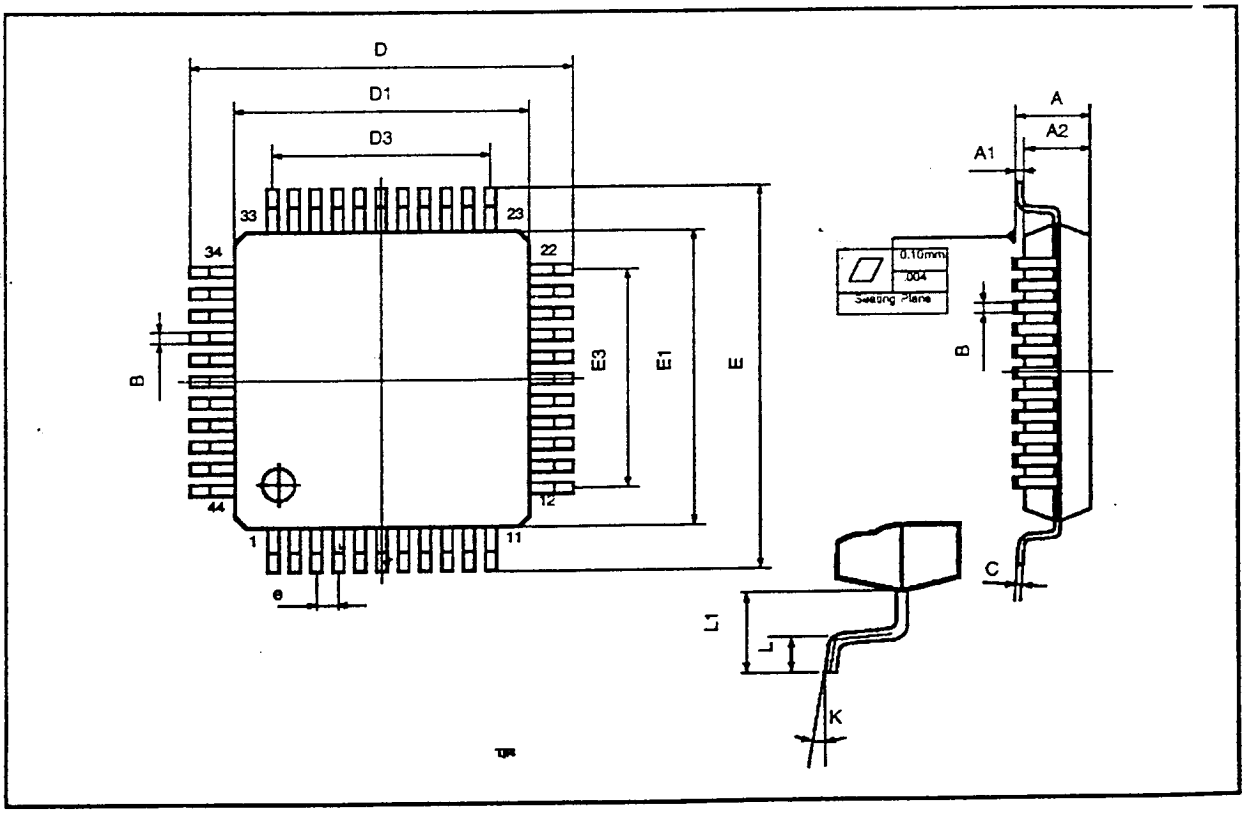
POWER SUPPLIES

While pins of ST5092 device are well protected against electrical misuse, it is recommended that the standard CMOS practise of applying GND before any other connections are made should always be followed. In applications where the printed circuit card may be plugged into a hot socket with power and clocks already present, an extra long ground pin on the connector should be used.

To minimize noise sources, all ground connections to each device should meet at a common point as close as possible to the GND pin in order to prevent the interaction of ground return currents flowing through a common bus impedance. A power supply decoupling capacitor of 0.1 µF should be connected from this common point to Vcc as close as possible to the device pins.

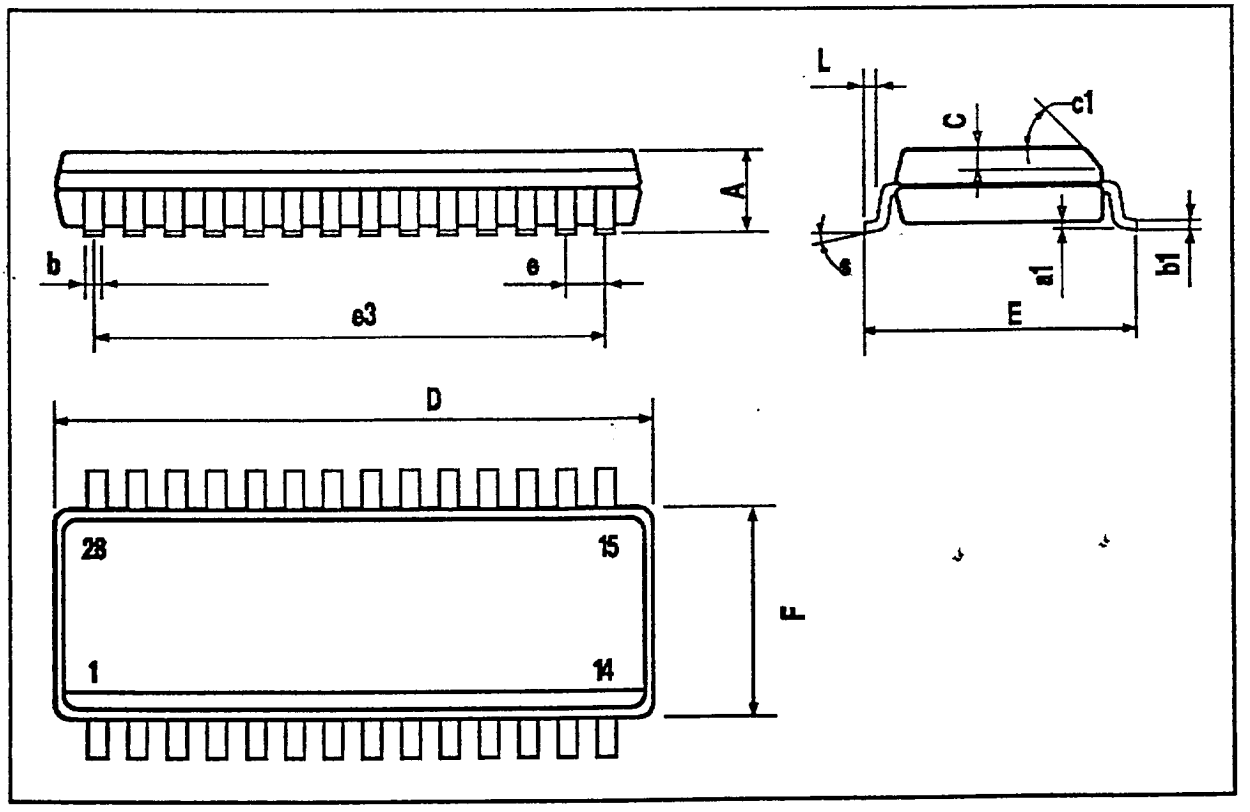
TQFP44 (10 x 10) PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.30	0.37	0.45	0.012	0.014	0.018
C	0.09		0.20	0.004		0.008
D		12.00			0.472	
D1		10.00			0.394	
D3		8.00			0.315	
e		0.80			0.031	
E		12.00			0.472	
E1		10.00			0.394	
E3		8.00			0.315	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
K	0°(min.), 3.5°(typ.), 7°(max.)					



SO28 PACKAGE AND MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.1		0.3	0.004		0.012
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.013
C		0.5			0.020	
c1	45° (typ.)					
D	17.7		18.1	0.697		0.713
E	10		10.65	0.394		0.419
e		1.27			0.050	
e3		16.51			0.65	
F	7.4		7.6	0.291		0.299
L	0.4		1.27	0.016		0.050
S	8° (max.)					

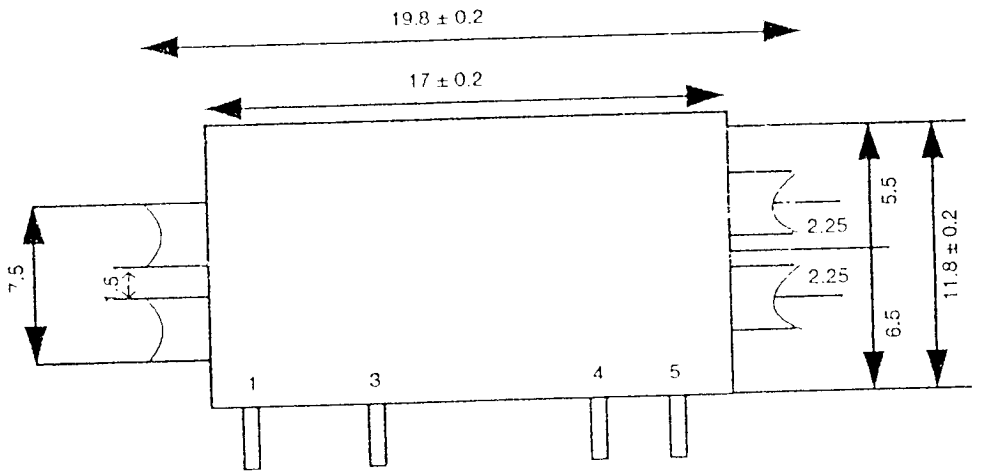


Power Amplifier

Rockwell Telecommunications

RI21002
CDMA/TDMA
HBT Power Amplifier

Outline Dimensions



* Note: Maximum thickness = 4.0mm
All dimensions in mm

Pin	Function
1	Input (RF)
3	DC Bias -A
4	DC Bias -B
5	Output (RF)

1. SCOPE. This specification establishes the electrical test requirements for the RI 21002 CDMA/FM Cellular Power Amplifier.

2. APPLICABLE DOCUMENTS

2.1 Documents Required by This Specification. The following documents to the extent indicated, form a part of this specification. In the event of any conflict between the requirements of this specification and the listed documents, the requirements of this specification shall govern.

SPECIFICATIONS

Rockwell International Corporation

GA-01102	ESD Protection Policy and Procedure, MTC
GA-01138	MTC; Test Equipment Certification and Qualification
GA-70050	Automated Test System, Wafer Lever Testing for Part Number 40026; Operating Instruction for (In work)
GA-70051	Automated Test System, Package Lever Testing for Part Number 40026; Operating Instruction for
GA-90010	GaAs IC, for CDMA/FM Cellular Power Amplifier, Test Equipment Specification for

OTHER DOCUMENTS

Rockwell International Corporation

PLDGA-70050	Program Listing Document for CDMA/FM Cellular Power Amplifier, Part Number 40026 Wafer Level Test (In work)
PLDGA-70051	Program Listing Document for CDMA/FM Cellular Power Amplifier, Part Number 40026 Package Level Test

Military

DOD-HDBK-263 Sect. 7.2.14 Relative Humidity	Electrostatic Discharge Control Handbook for Protection of Electrical and Electronic Parts, Assemblies and Equipment (Excluding Electrically Initiated Explosive Devices)

2.2 Documents Calling Out This Specification. In the event of any conflict between the requirements of this specification and documents calling out this specification, the requirements of the document calling out this specification shall take precedence.

DRAWINGS

Rockwell International Corporation

40126-510	Gallium Arsenide Integrated Circuit, for CDMA/FM Cellular Power Amplifier, Assembly of

3. REQUIREMENTS

3.1 Equipment. Acceptably precise results are contingent upon the use of the equipment specified in test equipment specification, GA-90010.

3.2 Materials. Acceptably precise results are contingent upon the use of the materials specified in GA-90010.

3.3 General Requirements. Test requirements for Final Packaged Device are listed in Section 6.

3.3.1 Absolute Maximum Ratings. At no time during testing shall the devices be subjected to conditions which are more severe than those listed below:

Supply Voltage (VDD):	-0.5 Vdc to +6.5 Vdc
Ambient Operating Temperature Range:	-30°C to +110°C
Continuous RF Input Power:	+17 dBm
Storage Temperature Range:	
Die and Wafer:	+25°C ± 20°C
Packaged Device:	-30°C to +125°C
Power Dissipation (if not otherwise specified)	
Total @ 110°C case:	2.50 W max

3.3.2 Environmental Conditions. Unless otherwise specified, operations required by this specification shall be performed at an ambient temperature of 25 ± 5°C, and a relative humidity of 40-60%.

3.3.3 Records of Data. Test data will be recorded as specified in GA-70050 and GA-70051. Required data is to be provided by tester printout when practical. Any suitable form may be used when a data printout is not available.

3.3.4 Measurements. Specification limits are to be considered absolute, regardless of the number of decimal places and are to be used as though they were continued with zeros.

3.3.4.1 Voltages. All voltage measurements are with reference to ground (GND). Measured values for voltage may be considered absolutely accurate when determining if a measured value is within specification limits.

3.3.4.2 Currents. Currents flowing into the device shall be recorded as positive currents and currents flowing out of the device shall be recorded as negative currents. Measured values of current may be regarded as absolutely accurate when determining if a measured value is within specification limits.

3.4 Detailed Requirements. Required electrical tests for wafer probe, interim electrical, and final electrical are defined in Table II. Prototype parts shall, at minimum, pass the same tests that were used at wafer probe.

3.4.1. All discrepancies shall be recorded in the test log and shall be dispositioned by Rockwell International Quality Assurance.

3.4.2 Electrical Tests. The test program shall provide for performing the tests shown in Section 6. Selected subgroups shall be performed at wafer probe, final electrical test as defined by Section 6.

4. QUALITY ASSURANCE PROVISIONS

4.1 Certification. Test certification shall be performed to assure compliance with the requirements of Section 3 and GA-01138.

4.2 Tests. All tests shall be performed using GA-70050 or GA-70051 with a test program which implements the requirements of Section 3. The sequence of tests is optional unless otherwise specified.

5. PREPARATION FOR DELIVERY. This section not applicable to this specification.

6. TABLES

Table I. List of Part Types Covered by this Specification

Spec.	Wafer P/N	Pkg P/N	Assembly Spec	Test OIS	Applicable Tables
RI 21002	40026	40026-21, -31, -41, -51, -61, -81, -111	40126-510	GA-70050 (In work), GA-70051	II, III

6. TABLES (continued)

Table II. CDMA/FM Cellular Power Amplifier - TESTS

Parameter	Freq. (MHz)	Power (dBm)	Vcc (V)	Specification	Test Method
Gain (small signal, Digital Mode)	836.5	Po = +1	5.0	27.5 -29.75 dB	ATE
Gain Variation over Frequency	824 - 849	Po = +1	5.0	± 0.5 dB	ATE
Gain Variation over Temperature	836.5	Po = +1	5.0	0 to -0.05 dB/C	QUAL
Gain Linearity	836.5	+1 ≤ Po ≤ 28	5.0	-1 to +1.5 dB	ATE
Noise Power	836.5	Po = 28	5.0	≤ -136 dBm/Hz	ATE
Input Impedance	836.5	Po = +7	5.0	≤ 2.2:1	ATE
Stability				Spurious < -70 dBc	QUAL
Harmonics (2 Fo & 3 Fo)	836.5	Po = 32	5.0	≤ -30 dBc	ATE
Analog Mode Po	836.5	Po = 32	5.0	Pin ≤ 5.0 mW	ATE
Analog Mode Efficiency	836.5	Po = 32	5.0	≥ 40% (bin ≥45%)	ATE
Digital Mode Efficiency	836.5	Po = 28	5.0	≥ 29%	ATE
		Po = 10	5.0	≥ 1%	ATE
Adjacent Channel Power Rejection	836.5	Po = 28	5.0	Offset ≥ ± 885 kHz ≥ 28 dBc	ATE
CDMA Waveform		Po = 28	5.0	Offset ≥ ± 1.98 MHz ≥ 41 dBc	ATE
Noise Figure	836.5		5.0	≤ 8 dB	ATE

Voltage Controlled Oscillator

№ HHK-BVCB511

Mar. 24. 1997

SPECIFICATIONS OF VOLTAGE CONTROLLED OSCILLATOR

P/N : VC-3R3A30-0967

FUJITSU TOWA ELECTRON LIMITED

SPECIFICATIONS OF VOLTAGE CONTROLLED OSCILLATOR	No	SHEET 1 OF 8 HHK-BVCB511

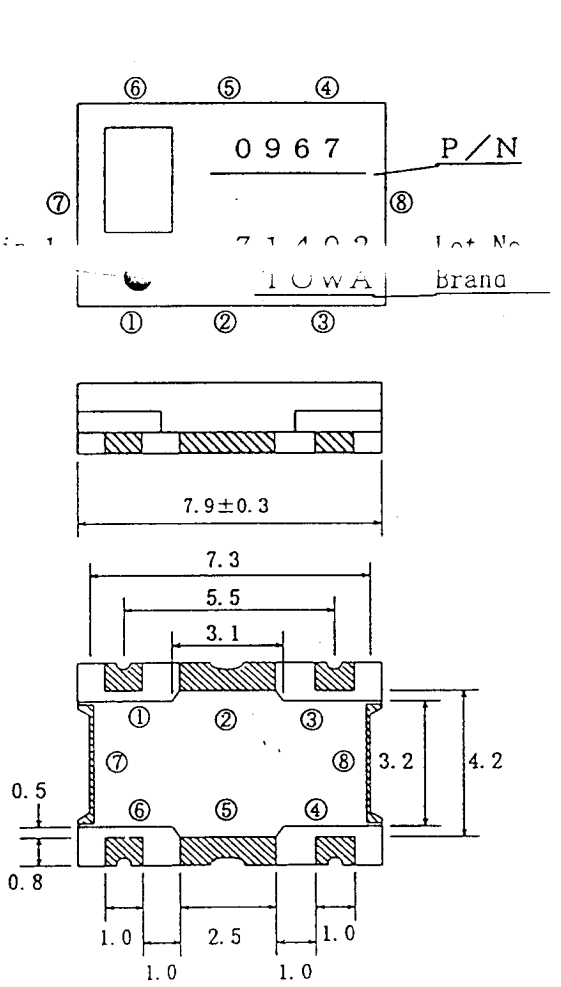
1. Applications

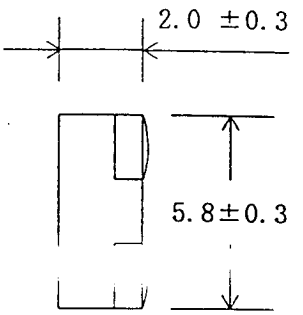
This document specifies a Voltage Controlled Oscillator of 900MHz band.

2. Product

VC-3R3A30-0967

3. Labeling and pin allocation





Pin allocation	
①	Voltage Control
②	GND
③	Supply Voltage
④	Output
⑤	GND
⑥	GND
⑦	GND
⑧	GND

Unit:mm

Figure. 1

Revision No.	Date	Revision	Approved by

Drawn by	Checked by	Approved by	Date
R. Matsuo	K. Iyori	T. Koizumi	Mar. 24, 1997

SPECIFICATIONS OF VOLTAGE CONTROLLED OSCILLATOR	No	SHEET 2 OF 8 HHK-BVCB511

4. Absolute Maximum Ratings <Table. 1>

Item	Symbol	Value	Unit
Supply Voltage	Vcc	+ 7.0	V
Operating Temp.	Topr	−30 ~ +80	℃
Storage Temp.	Tstg	−40 ~ +90	℃
Storage Humidity	Hstg	5 ~ 95	%

5. Electrical Test and Measurement Set-Up
5−1 Electrical Test <Table. 2>

Ta = 25 ± 3℃
*Ta = −30 ~ +80℃

No.	Item	Conditions		Specifications MIN	TYP	MAX	Unit	Method
1	Current Consumption Icc	Vcc=3.35V Vt =1.7 V				6.0 * 6.4	mA	Figure .2
2	Frequency at 0.7V fmin	Vcc=3.35V Vt =0.7 V				*954.0	MHz	"
3	Frequency at 2.7V fmax	Vcc=3.35V Vt =2.7 V		*980.0			MHz	"
4	Voltage Sensitivity SVt	(fmax-fmin)/2		* 21.0	25.0	* 28.0	MHz /V	"
5	Output Level Po	Vcc=3.35V Vt =1.7 V		-5.0 * -6.0	-2.5	0 * +1.0	dBm	"
6	C/N	Vcc=3.35V Vt =1.7 V	offset= 1kHz	* 70.0			dBc /Hz	"
			offset=10kHz	*100.0			dBc /Hz	"
			offset=30kHz	*110.0			dBc /Hz	"
			offset=60kHz	*115.0			dBc /Hz	"
7	Harmonic Attenuation	Vcc=3.35V, Vt=1.7V 2nd, 3rd				*-10.0	dBc	"
8	Spurious Level	Vcc=3.35V Vt =1.7 V				*-70.0	dBc	"

SPECIFICATIONS OF VOLTAGE CONTROLLED OSCILLATOR	No	SHEET 3 OF 8 HHK-BVCB511

No	Item	Conditions	Specifications			Unit	Method
			MIN	TYP	MAX		
9	Pushing Δf/ΔVcc	Vcc=3.35±0.25V Vt =1.7 V			*± 800	kHz	Figure .2
10	Pulling	Vcc=3.35V, Vt=1.7V VSWR=2 all phase			*±1000	kHz	"
11	Thermal Drift Δf/ΔT	25℃±55℃			*±3000	kHz	"

5－2 Measurement Set-Up

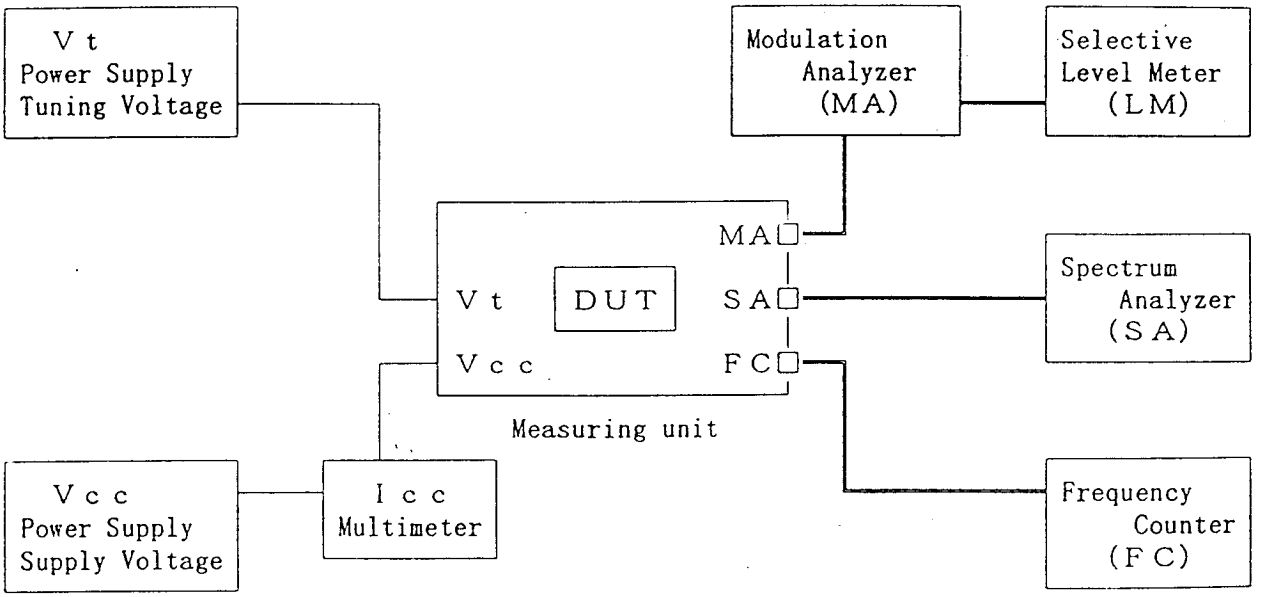


Figure. 2

*Measurement set up of C／N

- MA
  - HPF : 300 Hz
  - LPF : 200kHz
  - MEASUREMENT : FM
- LM
  - f : 1kHz, 10kHz, 30kHz, 60kHz
  - SLM(BW) : 3.1kHz

SPECIFICATIONS OF VOLTAGE CONTROLLED OSCILLATOR	No	SHEET 4 OF 8 HHK-BVCB511

6. Reliability Test

<Table. 3>

No	Item	Conditions and Method	Evaluation
1	High Temperature Test	Temp. +85℃± 2℃ Duration 96hrs ±2hrs When measured after 2 to 24 hours in normal conditions	Satisfied with electrical characteristics of 5-1 :Table 2. Suffer no physical damage.
2	Low Temperature Test	Temp. −30℃± 3℃ Duration 96hrs ±2hrs When measured after 2 to 24 hours in normal conditions	
3	High Temperature High Humidity Test	Temp. +60℃± 2℃ Humi. 90～95%RH Duration 96hrs ±2hrs When measured after 2 to 24 hours in normal conditions	
4	Temperature Cycle	-30℃± $^{3}_{5}$℃～ +25℃～ +85℃± $^{3}_{5}$℃～ +25℃ (30min) (5min) (30min) (5min) 10 Cycles Each cycle being 30 minutes minimum (-30℃ ,+85℃), and within 5 minutes (+25℃). When measured after 2 to 24 hours in normal conditions	
5	Resistance to Soldering Heat	Temp. 260℃± 5℃ Duration 10sec ±2sec Method Put a ceramic substrate on a solder bath, on top the D.U.T. When measured after 2 to 24 hours in normal conditions	
6	Shock	Height 75cm± $^{5}_{0}$cm Position Three perpendicular planes. Times 1 each Method The D.U.T free-falls(1G) on a Wood(maple) surface(3cm-thick min).	
7	Vibration	Amplitude 1.5mm ±0.225mm Frequency 10±1Hz ～55±1.1Hz ～10±1Hz Cycle 1min per cycle Position Three perpendicular planes. Duration 2hrs each	
8	Solderability	Temp. 230℃± 5℃ Duration 3sec± $^{2}_{0}$sec Method Dip the D.U.T terminals in a solder bath.	At least 90% of each terminals shall be covered with new solder.

SPECIFICATIONS OF VOLTAGE CONTROLLED OSCILLATOR	No	SHEET 8 OF 8 HHK-BVCB511

9. Other information

9－1 Environmental

The product specified in this specification does not use any kind of Ozone depletion materials, dangerous or poisonous substances regulated by low in the fabrication process.

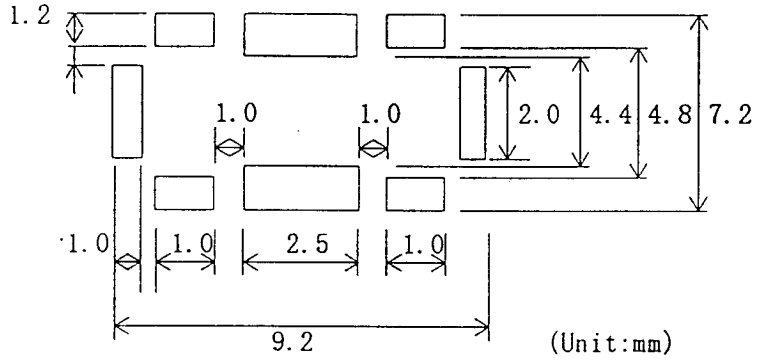
9－2 Handling information

Please do not apply any kind of over stress to the product during mounting or do not bend or twist the shield case which may cause wrong oscillation frequency.

9－3 Modification of specification

If necessary, we will change the specification with an agreement with purchaser.

9－4 Recommended PCB Land Pattern



9－5 Lot.Number (date code) Reading Method

7 1 4 0 2

- Production Facility Code: 1 ～ 4 Tohoku Towa (Japan Factory)
  5 Su-zhou Towa (China Factory)
- Day of Week (Mon:0 ～ Sun:6)
- Week code
- Year code (Last digit of year)

VC-TCXO

No.	TA970730

4. ELECTRICAL CHARACTERISTICS

(Ta=25±1℃, Vcc=3.3±0.165V, Vcon=1.5±0.03V, RL=10kΩ/10pF, unless otherwise specified.)

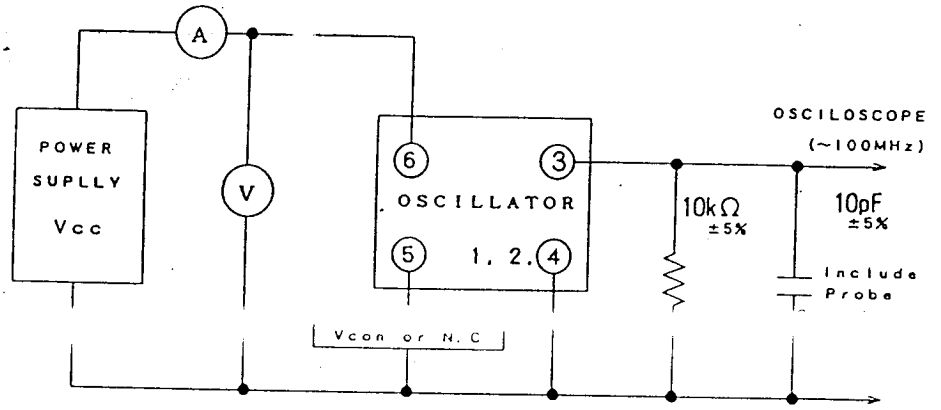
ITEMS	MIN.	TYP.	MAX.	UNIT	CONDITIONS	REMARKS
NOMINAL FREQUENCY	——	19.68	——	MHz		
OUTPUT VOLTAGE	0.8	——	——	Vp-p	LOAD 10KΩ/10pF	
POWER SUPPLY CURRENT	——	——	1.5	mA	WITHOUT LOAD	
INITIAL TOLERANCE	-0.5	——	0.5	ppm	LOAD 10KΩ/10pF Vcon=1.5V	
FRF after 1 REFLOW (REF INITIAL)			1.0	ppm	LOAD 10KΩ/10pF Vcon=1.5V	
FREQUENCY STABILITY	-2.0	——	2.0	ppm	TEMP -30~80℃	
	-0.2	——	0.2	ppm	LOAD 10pF ±10% 10KΩ ±10%	
	-0.3	——	0.3	ppm	Vcc=3.3V±5%	
FREQUENCY AGING RATE	-1.0	——	1.0	ppm/Y	Vcc=3.3±0.1V Ta=25±1℃	ONE YEAR
VOLTAGE CONTROL RANGE	-7.5	——	-4.45	ppm	Vcon=0.5V	VS INITIAL FREQUENCY (Vcon=1.5V)
	4.45	——	7.5	ppm	Vcon=2.5V	
HARMONICS	——	——	-5	dBc		
PHASE NOISE	——	——	-85	dBc/Hz	FO±30Hz	
	——	——	-120	dBc/Hz	FO±100Hz	
	——	——	-125	dBc/Hz	FO±1KHz	

REV.	DESCRIPTION	DATE	DRAWN	CHECKED	CHECKED	APPROVED

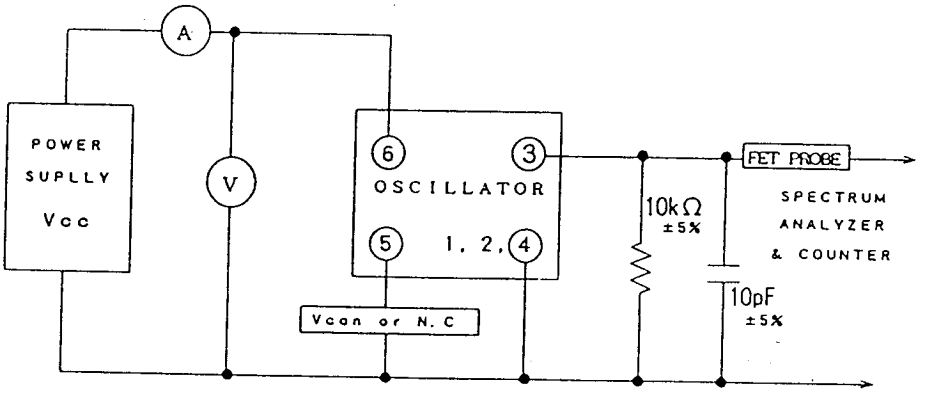
No.	TA970730

5. TEST CIRCUIT

5-1. TEST CIRCUIT (1)
(AMPLITUDE)



5-2. TEST CIRCUIT (2)
(HARMONICS & FREQUENCY)

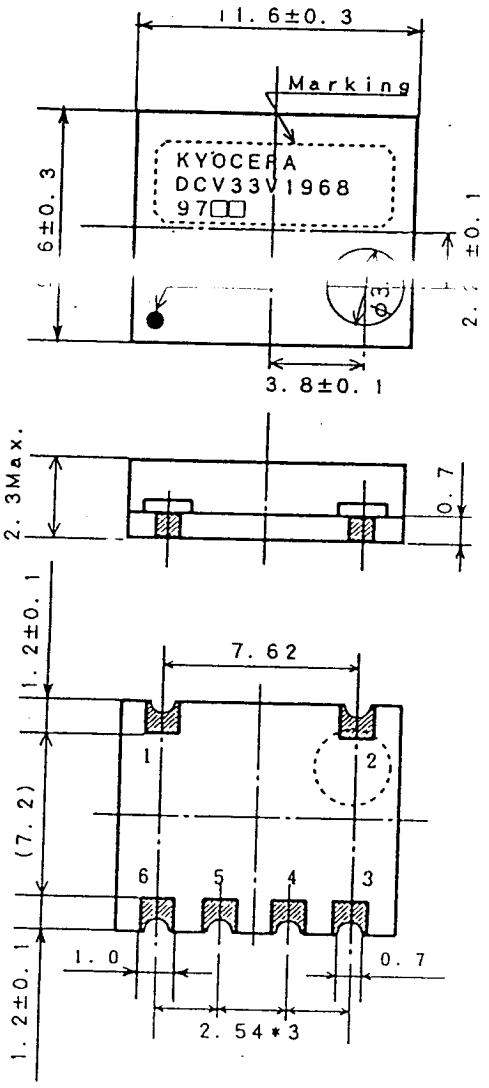


REV.	DESCRIPTION	DATE	DRAWN	CHECKED	CHECKED	APPROVED

No.	TA970730

6. DIMENSIONS&APPEARANCE

6-1. OUTLINE



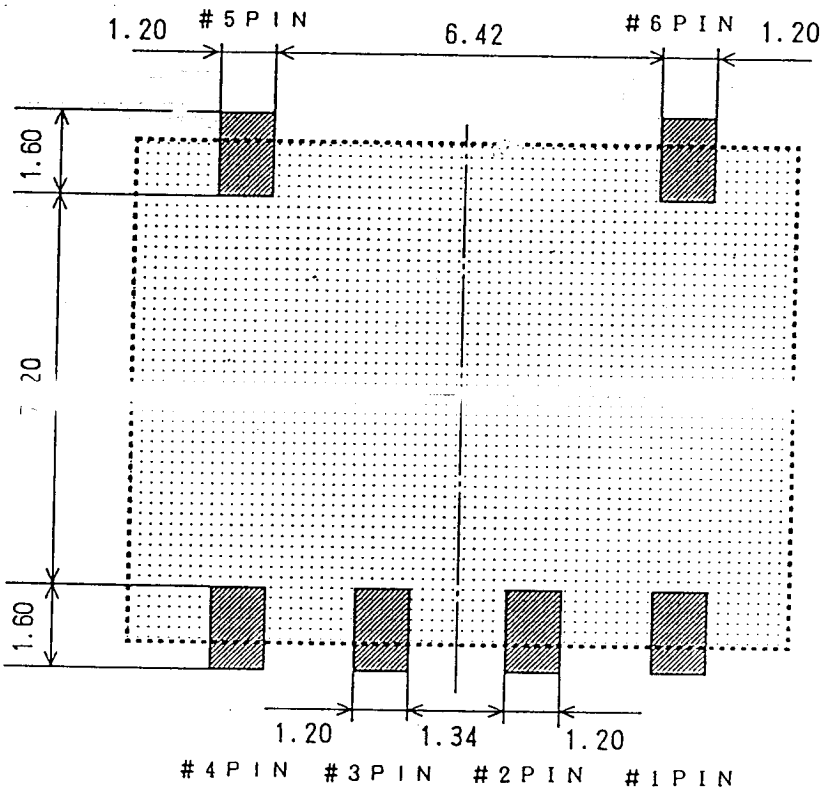
	PIN CONNECTION
1	GND/CASEGND
2	GND/CASEGND
3	OUTPUT
4	GND/CASEGND
5	Vcon or N.C
6	+Vcc

DIMENSION: [mm]

REV.	DESCRIPTION	DATE	DRAWN	CHECKED	CHECKED	APPROVED

No.	TA970730

6-2. RECOMMENDED LAND PATTERN (TOP VIEW)



DIMENSION:[mm]

REV.	DESCRIPTION	DATE	DRAWN	CHECKED	CHECKED	APPROVED

No.	TA970730

7. MARKING SPECIFICATION

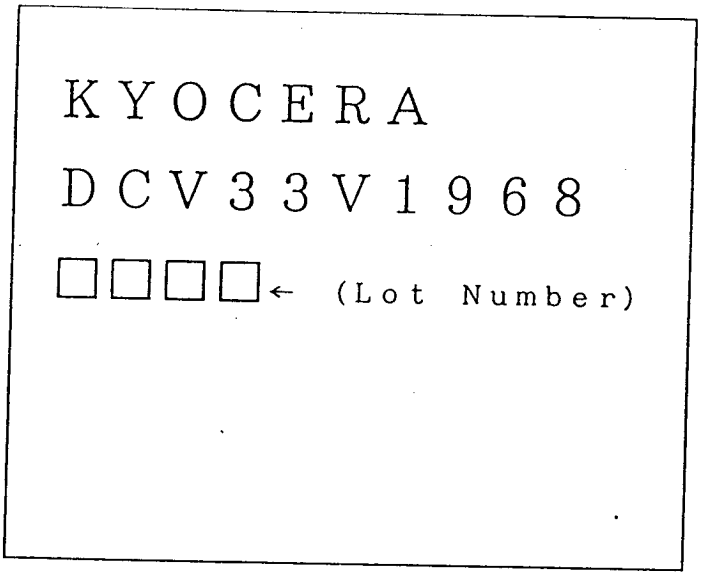
7-1. MANUFACTURING DATE CODE

Manufacturing date (year & week) is indicated below.

EXAMPLE 1997 01st week --- 「9701」
1997 02nd week --- 「9702」
1997 03rd week --- 「9703」
:
:
1997 52th week --- 「9752」
1998 01st week --- 「9801」

7-2. MARKING

KYOCERA,Part number,Frequency,Production lot number



REV.	DESCRIPTION	DATE	DRAWN	CHECKED	CHECKED	APPROVED

Upconverter

NEC

バイポーラ アナログ集積回路
Bipolar Analog Integrated Circuits

μPC8106T, μPC8109T

セルラ・コードレス電話用1.9 GHzアップコンバータIC

μPC8106T, 8109Tはセルラ・コードレス電話の送信段用アップコンバータとして開発されたシリコン・モノリシックICです。3 Vで動作し、ミニパッケージのためセットの低消費電力・小形化が可能です。

本製品は、当社独自のシリコン・バイポーラプロセス「NESAT™III」(f_T = 20 GHz)により生産しています。本プロセスはダイレクト・シリコン窒化膜や金電極構造を採用しています。この構造はチップの耐湿性、耐食性に優れ、良好な電流特性、高周波特性を有します。これにより信頼性、電気的特性に優れた高品質のICを実現しています。

特　徴

- 高周波数帯域が広い：f_{RFmax} = 0.8 GHz ～ 1.9 GHz, f_{IFmax} = 100 MHz ～ 400 MHz
- 電源電圧：2.7 ～ 5.5 V
- 高密度・面実装が可能：6ピン・ミニモールド
- 低消費電流：9 mA：μPC8106T, 5 mA：μPC8109T
- キャリアリークが少ない：ダブル・バランスド・ミキサ
- パワーセーブ機能を内蔵

応　用

- PHP, PDC：μPC8106T
- アナログセルラ, CT2：μPC8109T

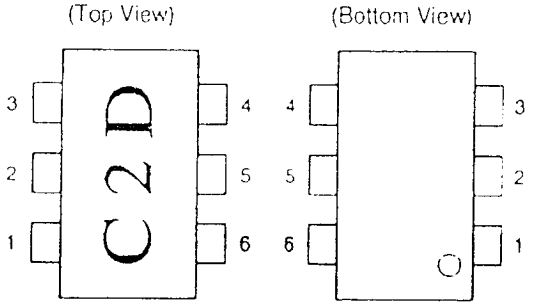
オーダ情報

オーダ名称	パッケージ	包装形態	品質水準
μPC8106T-E3 μPC8109T-E3	6ピン・ミニモールド	8 mm幅エンボス式テーピング。 1, 2, 3ピン送り穴方向。 3 k個／リール。	標準（一般電子機器用）

備考　評価用サンプルのオーダについては，販売員にお問い合わせください（名称：μPC8106T, μPC8109T）

品質水準とその応用分野の詳細については当社発行の資料「NEC 半導体デバイスの品質水準」(IEI-620)をご覧ください。

端子接続図



捺印は μPC8106T：C2D
μPC8109T：C2G

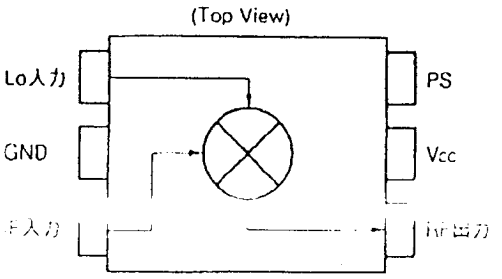
端子番号	機能(2品種共通)
1	IF入力
2	GND
3	Lo入力
4	PS端子
5	Vcc
6	RF出力

製品系列一覧 (T_a = +25 °C, V_{CC} = 3.0 V, Z_L = Z_S = 50 Ω)

タイプ名	品 名	Vcc (V)	Icc (mA)	CG1 (dB)	CG2 (dB)	$P_{out,sat}1$ (dBm)	$P_{out,sat}2$ (dBm)	$OIP_3$1 (dBm)	$OIP_3$2 (dBm)
高IP_3	μPC8106T	2.7~5.5	9	10	7	−2	−4	+7	+6.5
低消費電流	μPC8109T	2.7~5.5	5	7	5	−6	−8	+5	+1.5

備考 主要項目のTYP.値。規格条件は電気的特性欄を参照

ブロック図 (2品種共通)

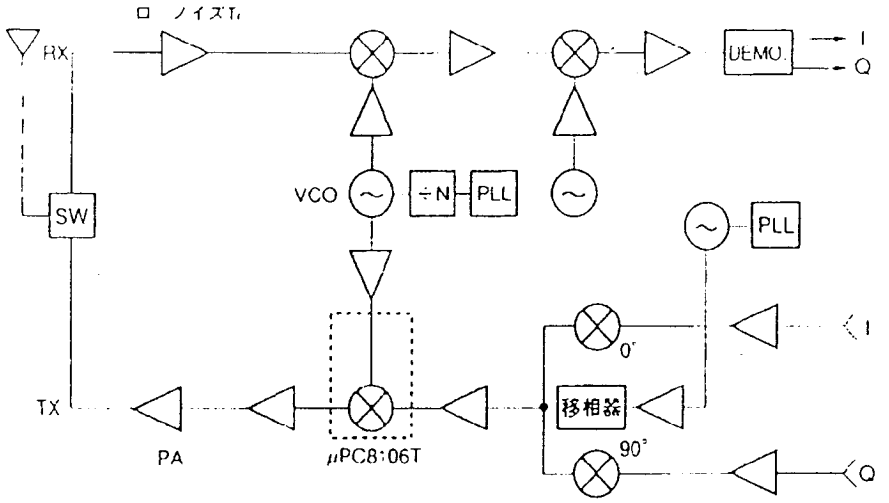


μPC8106T
・高IP_3：出力IP_3 = +7 dBm

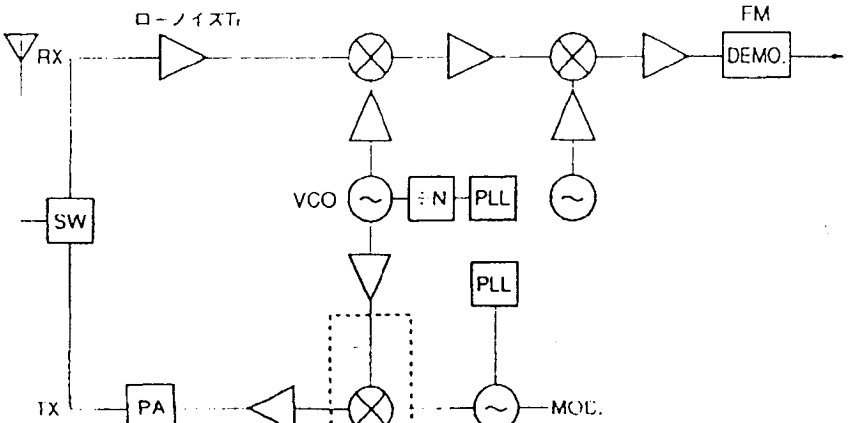
μPC8109T
・低消費電流：5 mA @3 V

システム応用例

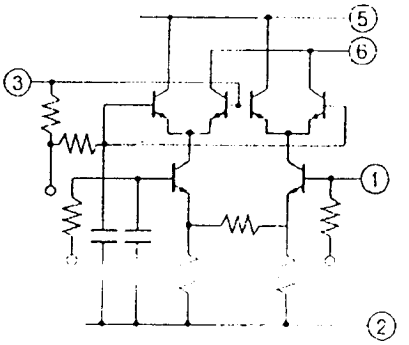
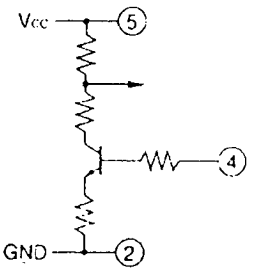
PHP



アナログセルラ



端子機能 μPC8106T, μPC8109T 共通

端子番号	端子名称	端子電圧 (V)	機能および説明	等価回路
1	IF_{input}	1.3	ミキサのIF入力端子で、高インピーダンス入力です。 ダブルバランス型ミキサによりキャリアリークの少ない良好な特性を有します。 また、プロセス・バラツキの影響を小さくする目的で対称な回路を採用しています。	
2	GND	0[注1]	GND端子です。グラウンド・パターンは最小インピーダンスになるよう十分広く取ってください。	
3	L_{input}	2.4	ローカル入力端子です。	
5	Vcc	2.7～5.5[注1]	電源電圧端子です。	
6	RF_{output}	-	RF出力端子です。オープンコレクタ出力です。ハイ・インピーダンスのため、L,Cで接続回路とマッチングを取ってください。	
4	PS	Vcc/GND[注1]	パワーセーブ端子です。 Vccで動作し、GNDでパワーセーブ状態(OFF)になります。	

注1 外部印加電圧

各端子電圧はVcc = 3.0 Vの場合

絶対最大定格

項目	略号	条件	定格	単位
電源電圧	V_{CC}	T_a = +25 °C	6.0	V
PS端子入力電圧	$V_{P/S}$	T_a = +25 °C	6.0	V
パッケージ許容損失	P_D	50 × 50 × 1.6 mm 全銅箔両面ガラスエポキシ基板実装時 T_a = +85 °C	280	mW
動作温度範囲	T_{opt}		−40～+85	°C
保存温度範囲	T_{stg}		−55～+150	°C

推奨動作範囲

項目	略号	MIN.	TYP.	MAX.	単位
電源電圧	V_{CC}	2.7	3.0	5.5	V
動作温度範囲	T_{opt}	−40	+25	+85	°C
ローカル入力レベル	P_{Loin}	−10	−5	0	dBm
RF出力周波数	f_{RFout}	0.4	−	1.9	GHz
IF入力周波数	f_{IFin}	100	−	400	MHz

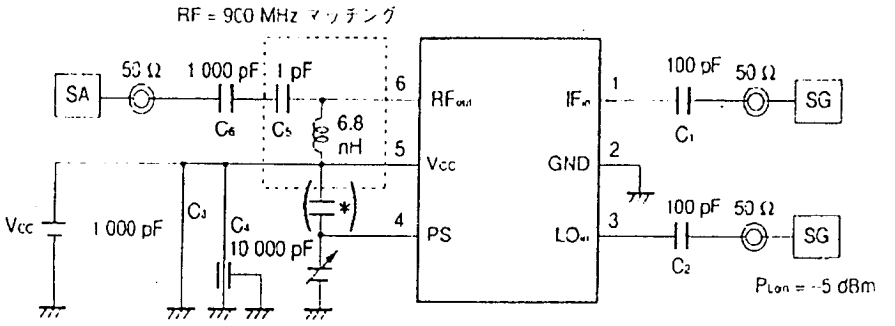
電気的特性 (T_a = +25 °C, V_{CC} = 3.0 V, 特に指定のない限り f_{IFin} = 240 MHz, P_{Loin} = −5 dBm, $V_{P/S}$≧2.7 V)

項目	略号	条件	μPC8106T			μPC8109T			単位
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
回路電流	I_{CC}	入力無信号時	4.5	9	13.5	2.5	5	8.0	mA
パワーセーブ時電流	$I_{CC(P/S)}$	$V_{P/S}$ = 0 V			10			10	μA
変換利得1	CG1	f_{RFout} = 0.9 GHz, P_{IFin} = −30 dBm	7	10	13	4	7	10	dB
変換利得2	CG2	f_{RFout} = 1.9 GHz, P_{IFin} = −30 dBm	4	7	10	2	5	8	dB
最大出力電力1	$P_{O(sat)1}$	f_{RFout} = 0.9 GHz, P_{IFin} = 0 dBm	−4	−2		−7.5	−5.5		dBm
最大出力電力2	$P_{O(sat)2}$	f_{RFout} = 1.9 GHz, P_{IFin} = 0 dBm	−6.5	−4		−10	−7.5		dBm

標準参考特性(T_a = +25 °C, V_{CC} = 3.0 V, 特に指定のない限り f_{IFin} = 240 MHz, P_{Loin} = −5 dBm, $V_{P/S}$≧2.7 V)

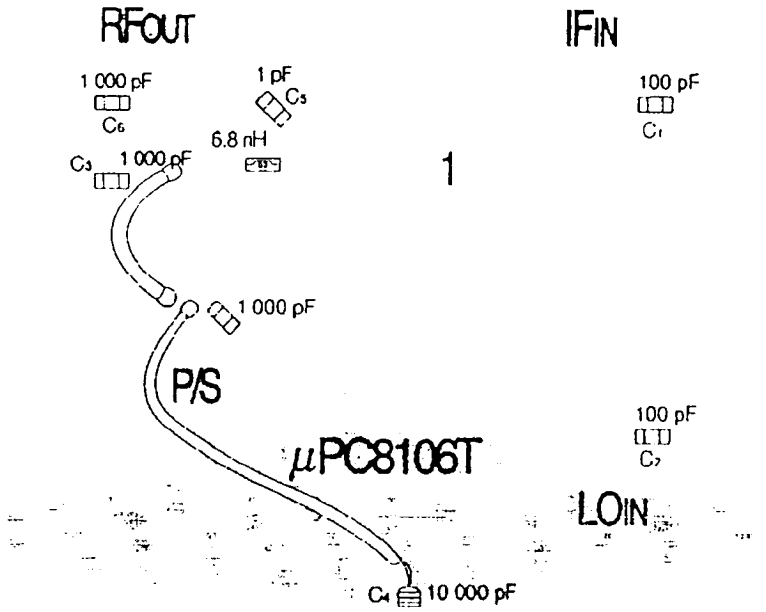
項目	略号	条件		参考値		単位
				μPC8106T	μPC8109T	
出力3次ひずみインタセプト・ポイント	$OIP_{3}1$	f_{IFin1} = 240.0 MHz f_{IFin2} = 240.4 MHz	f_{RFout} = 0.9 GHz	+7	+5	dBm
	$OIP_{3}2$		f_{RFout} = 1.9 GHz	+6.5	+1.5	
3次相互変調ひずみ1	$IM_{3}1$	f_{IFin1} = 240.0 MHz f_{IFin2} = 240.4 MHz P_{IFin} = −20 dBm	f_{RFout} = 0.9 GHz	31	29	dBc
3次相互変調ひずみ2	$IM_{3}2$		f_{RFout} = 1.9 GHz	30	28	dBc
SSB雑音指数	SSBNF	f_{RFout} = 0.9 GHz		8.5	8.5	dB

測定回路図1（RF 900 MHzの場合。2品種共通）



＊動作が安定しない場合に4ピン－5ピン間に100 pFの容量を挿入し，マッチングの再調整をしてください。

測定回路図1のプリント基板実装例



部品注

6.8 nH：LQP31A6N8J04（村田製作所殿製）

基板例注釈

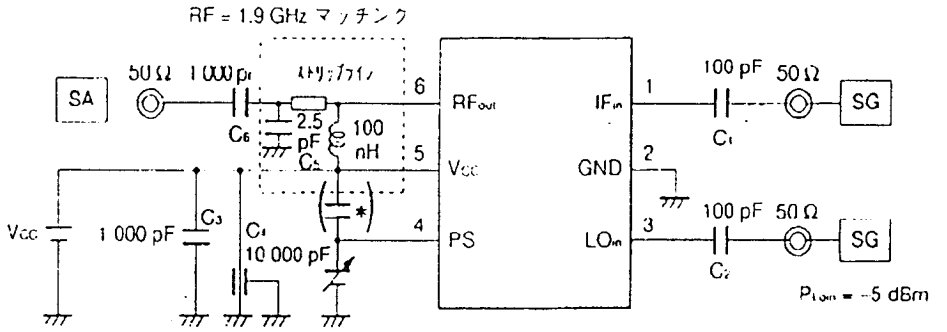
（＊1）35×42×0.4 mmポリイミド版に両面35 μm厚銅パターニング

（＊2）裏面GNDパターン

（＊3）パターニング面ハンダメッキ

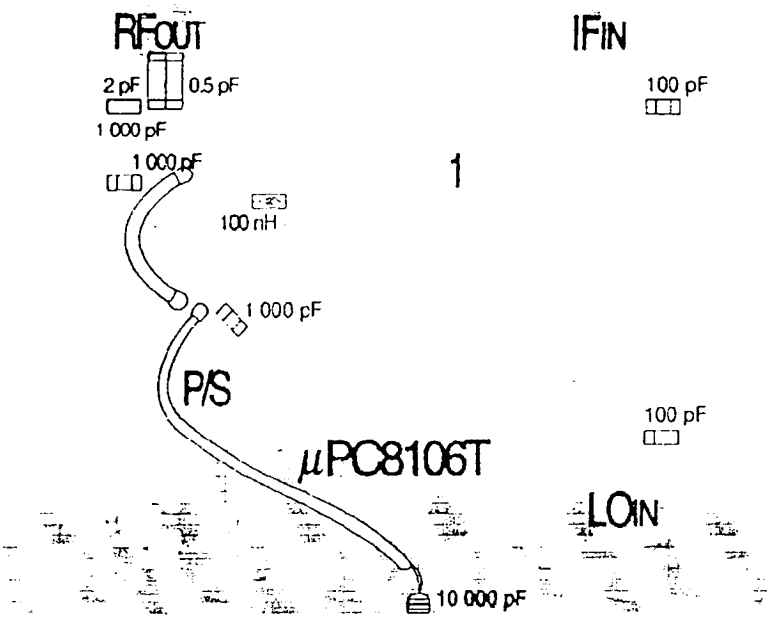
（＊4）○◯◯はスルーホール

測定回路図2（RF 1.9 GHzの場合，2品種共通）



＊動作が安定しない場合に4ピン－5ピン間に100 pFの容量を挿入し，マッチングの再調整をしてください。

測定回路図2のプリント基板実装例



部品注

100 nH：LQN1AR10J(K)04（村田製作所殿製）

基板例注釈

（＊1）35×42×0.4 mmポリイミド版に両面35 μm厚銅パターニング

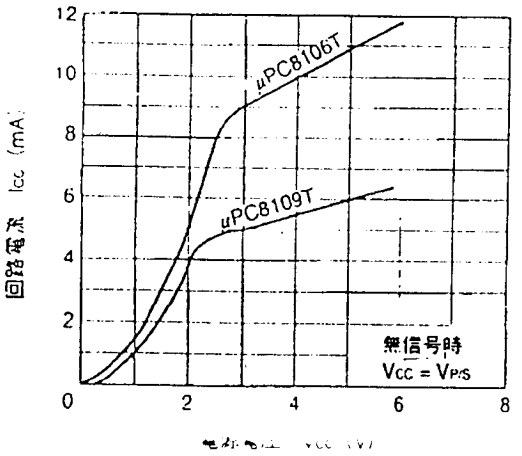
（＊2）裏面GNDパターン

（＊3）パターニング面ハンダメッキ

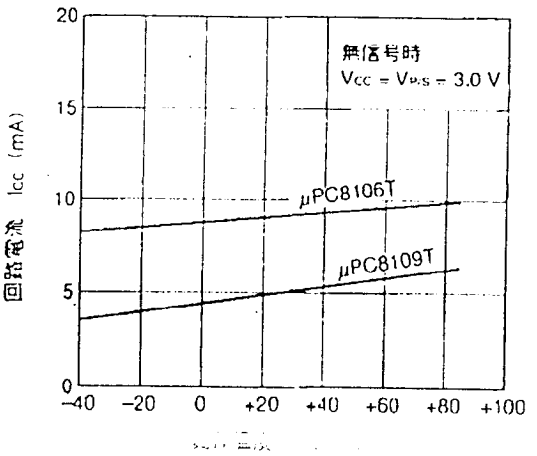
（＊4）o○○はスルーホール

特性曲線（Ta = +25 °C）特に指定のない限り，各周波数ごとの測定回路図1, 2による。

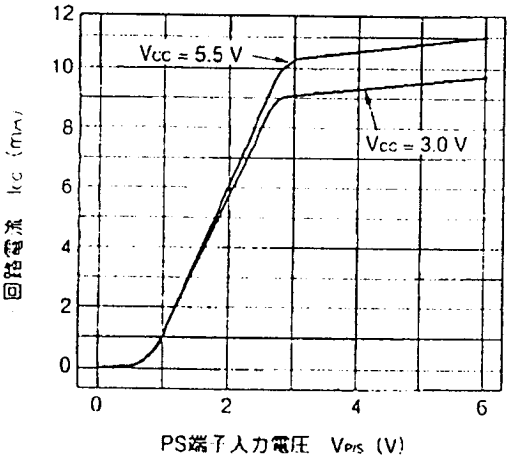
CIRCUIT CURRENT vs. SUPPLY VOLTAGE



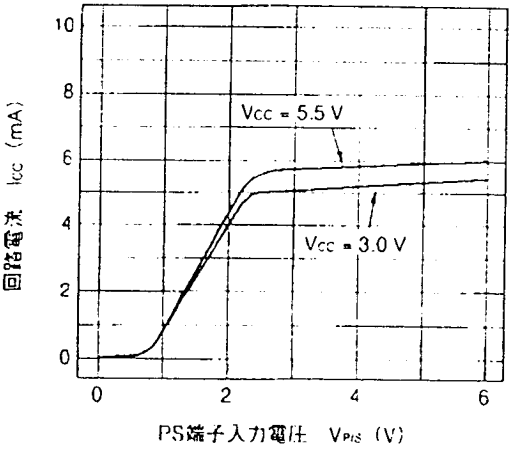
CIRCUIT CURRENT vs. TEMPERATURE



μPC8106T CIRCUIT CURRENT vs. PS PIN INPUT VOLTAGE

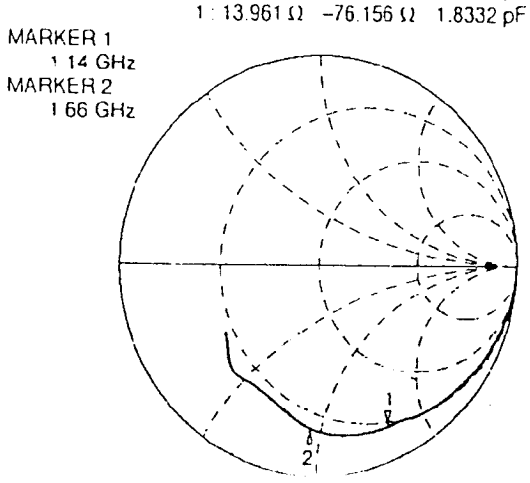


μPC8109T CIRCUIT CURRENT vs. PS PIN INPUT VOLTAGE

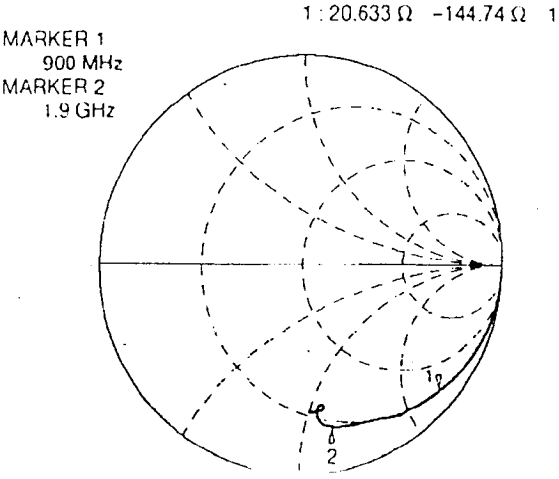


各ポートSパラメータ（V_{CC} = $V_{P/S}$ = 3.0 V）－2品種共通－

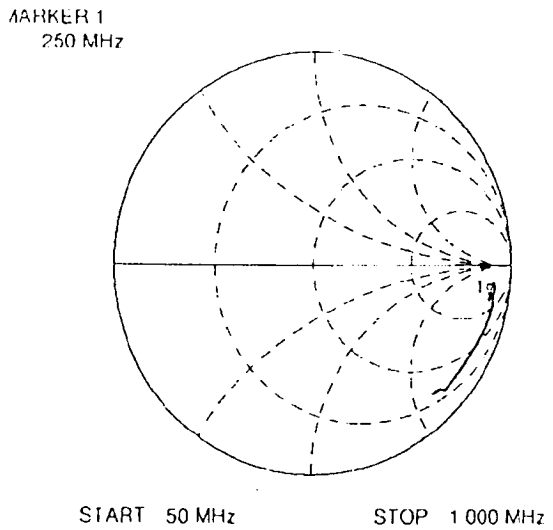
LOポート　2 : 12.050 Ω　−45.695 Ω　2.1780 pF
1 : 13.961 Ω　−76.156 Ω　1.8332 pF



RFポート（マッチングなし）　2 : 13.845 Ω　−77.34 Ω　1.0850 pF
1 : 20.633 Ω　−144.74 Ω　1.2218 pF

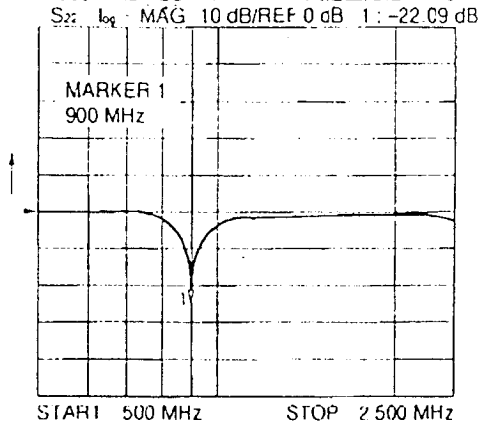


IFポート　1 : 154.64 Ω　−494.41 Ω　1.2876 pF

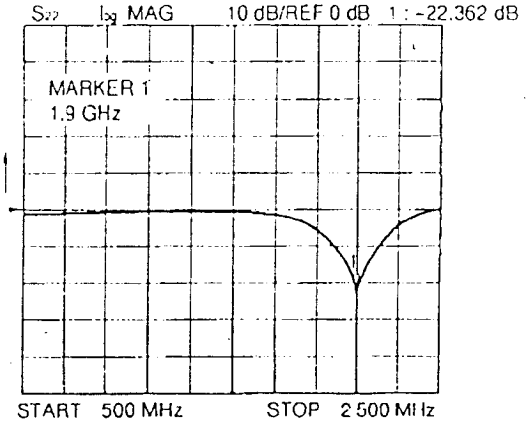


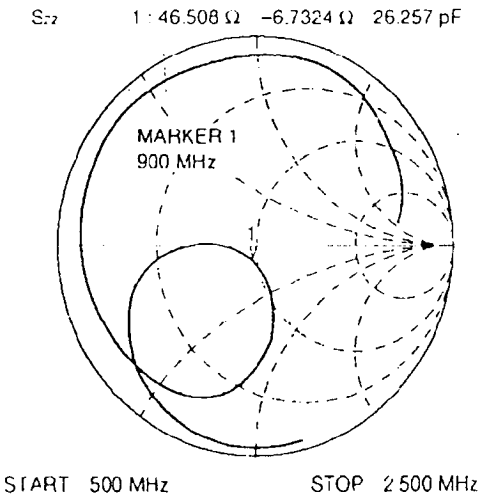
RF出力マッチング時のSパラメータ（V_{CC} = $V_{P/S}$ = 3.0 V）－測定基板による(2品種共通)－

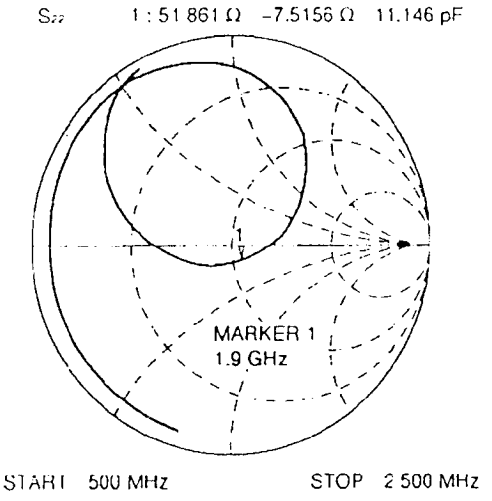
S_{22} : 900 MHz LCマッチング 測定回路図1による



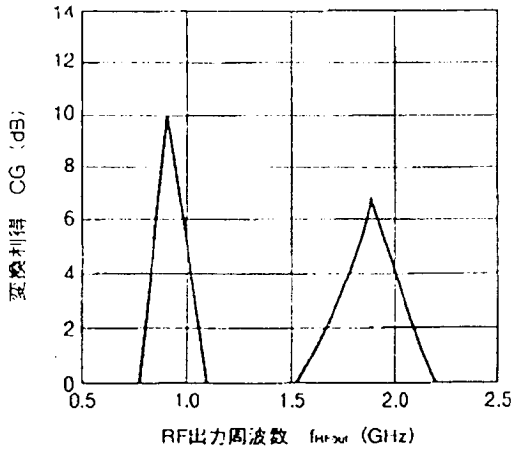
S_{22} : 1.9 GHz マッチング 測定回路図2による



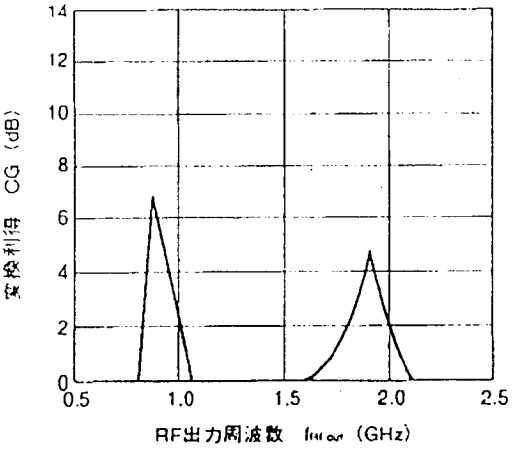




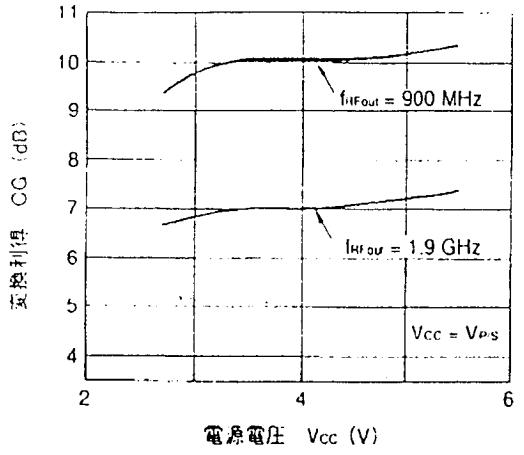
μPC8106T CONVERSION GAIN vs. RF OUTPUT FREQUENCY ON MATCHED TEST BOARD



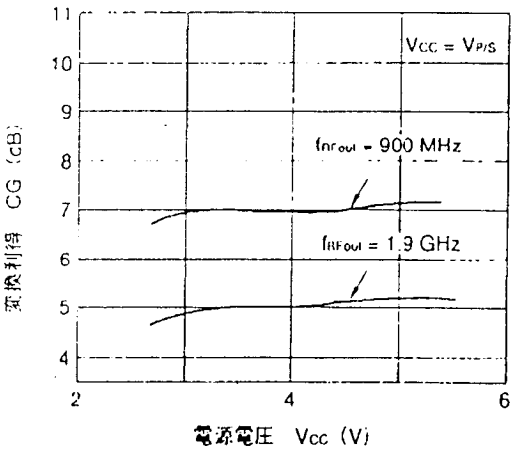
μPC8109T CONVERSION GAIN vs. RF OUTPUT FREQUENCY ON MATCHED TEST BOARD



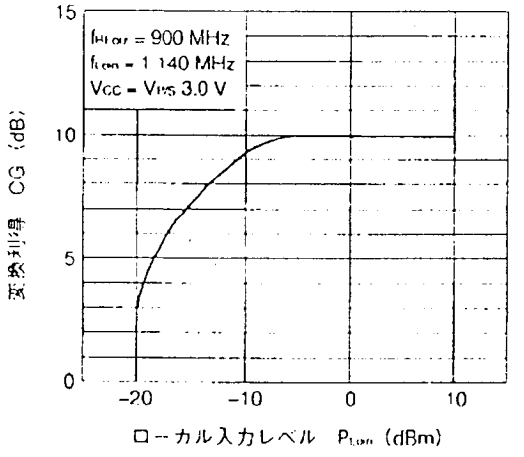
μPC8106T CONVERSION GAIN vs SUPPLY VOLTAGE



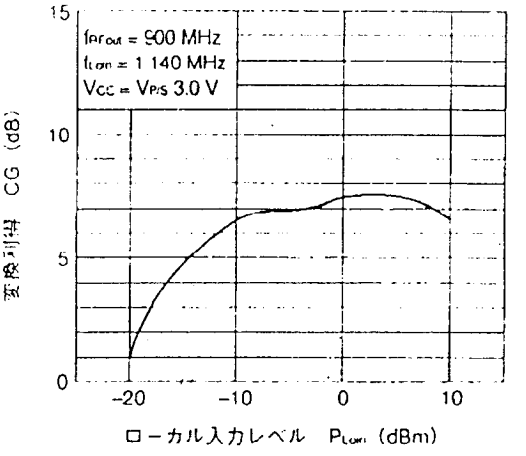
μPC8109T CONVERSION GAIN vs SUPPLY VOLTAGE



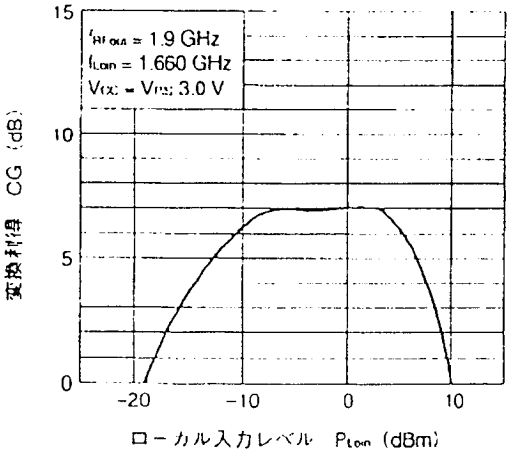
μPC8106T CONVERSION GAIN vs.



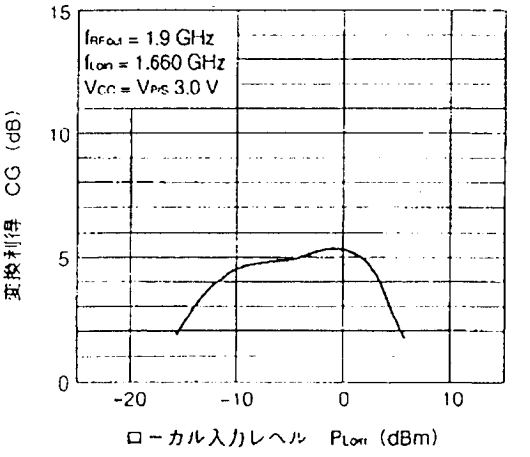
μPC8109T CONVERSION GAIN vs.



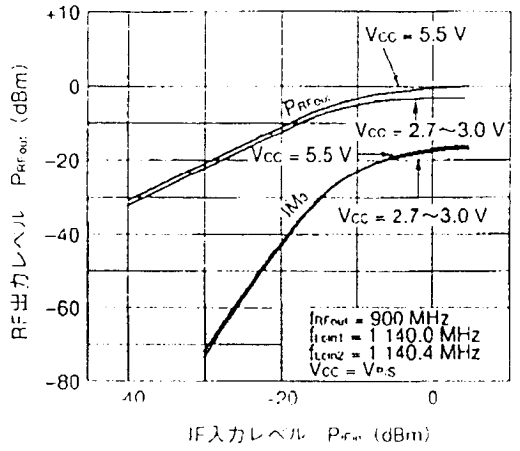
μPC8105T CONVERSION GAIN vs. LOCAL INPUT LEVEL AT RF 1.9 GHz



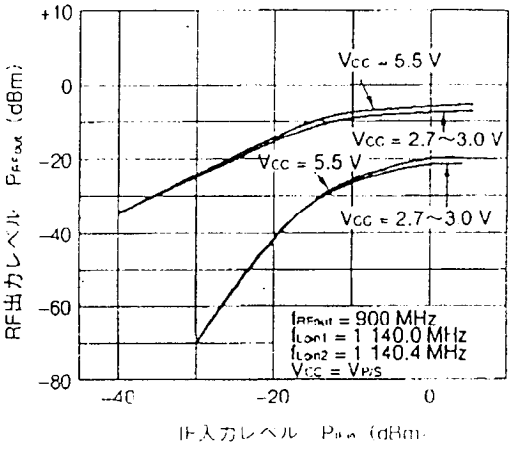
μPC8109T CONVERSION GAIN vs. LOCAL INPUT LEVEL AT RF 1.9 GHz



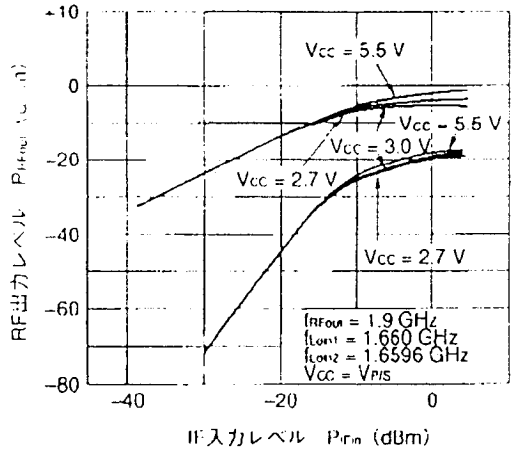
μPC8106T IM3 AND RF OUTPUT LEVEL
vs. IF INPUT LEVEL AT RF 900 MHz



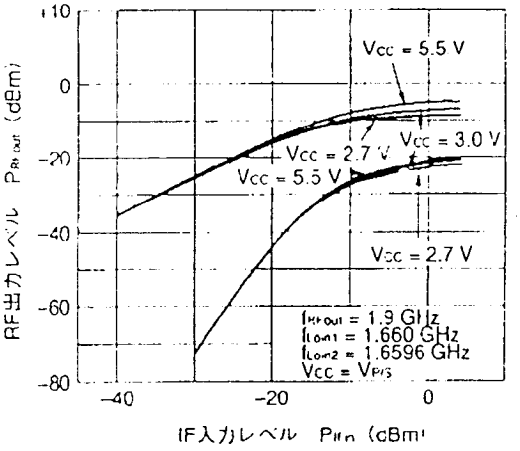
μPC8109T IM3 AND RF OUTPUT LEVEL
vs. IF INPUT LEVEL AT RF 900 MHz



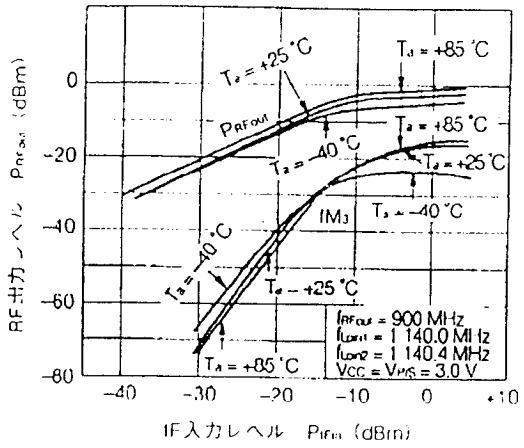
μPC8106T IM3 AND RF OUTPUT LEVEL
vs. IF INPUT LEVEL AT RF 1.9 GHz



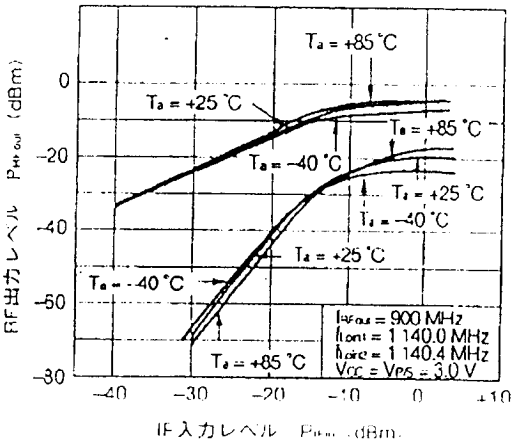
μPC8109T IM3 AND RF OUTPUT LEVEL
vs. IF INPUT LEVEL AT RF 1.9 GHz



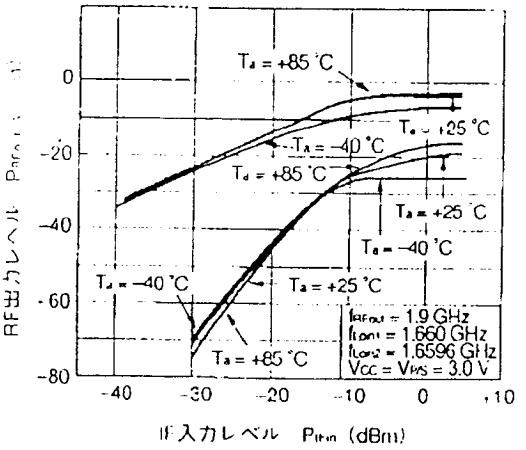
μPC8106T IM3 AND RF OUTPUT LEVEL
vs. IF INPUT LEVEL AT RF 900 MHz



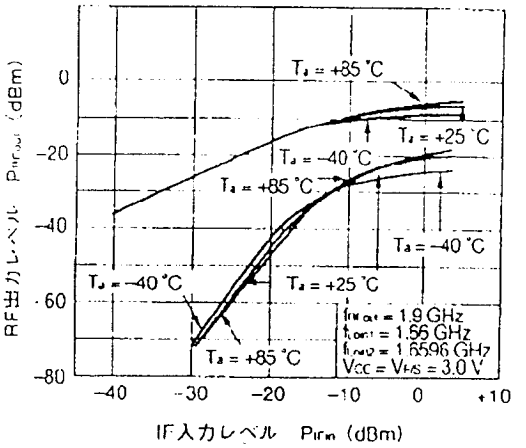
μPC8109T IM3 AND RF OUTPUT LEVEL
vs. IF INPUT LEVEL AT RF 900 MHz



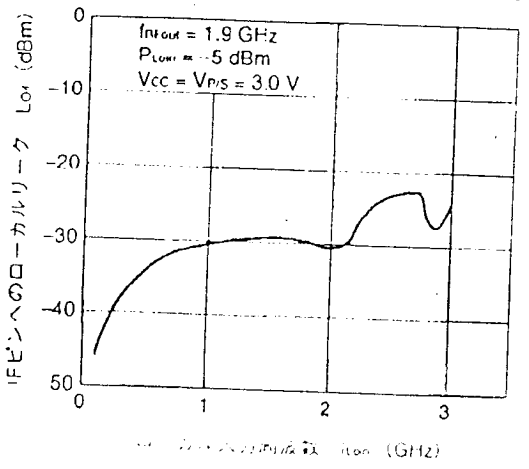
μPC8106T IM3 AND RF OUTPUT LEVEL
vs. IF INPUT LEVEL AT RF 1.9 GHz



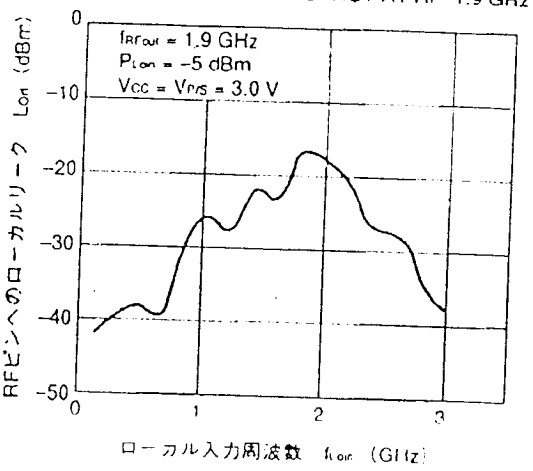
μPC8109T IM3 AND RF OUTPUT LEVEL
vs. IF INPUT LEVEL AT RF 1.9 GHz



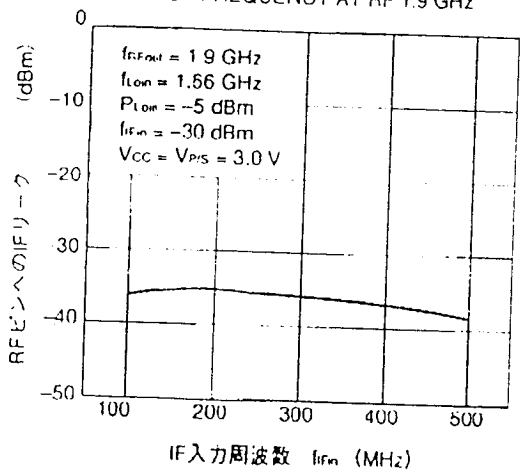
μPC8106T LOCAL LEAKAGE AT IF PIN vs.
LOCAL INPUT FREQUENCY AT RF 1.9 GHz



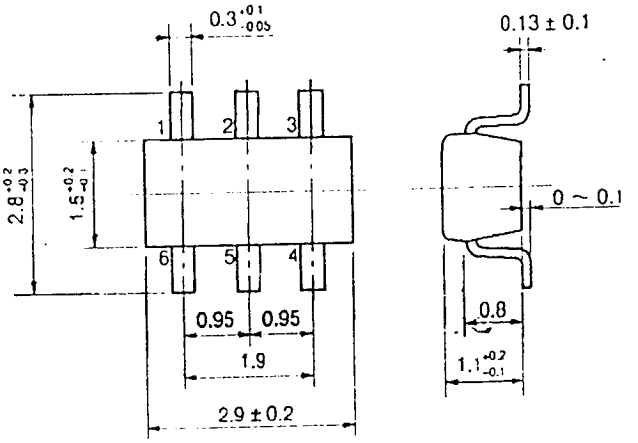
μPC8106T LOCAL LEAKAGE AT RF PIN vs.
LOCAL INPUT FREQUENCY AT RF 1.9 GHz



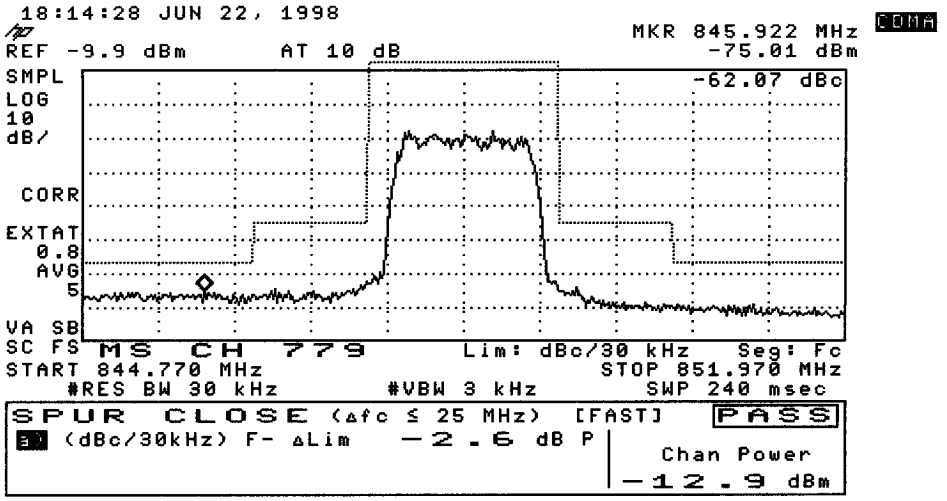
μPC8106T IF LEAKAGE AT RF PIN vs.
IF INPUT FREQUENCY AT RF 1.9 GHz

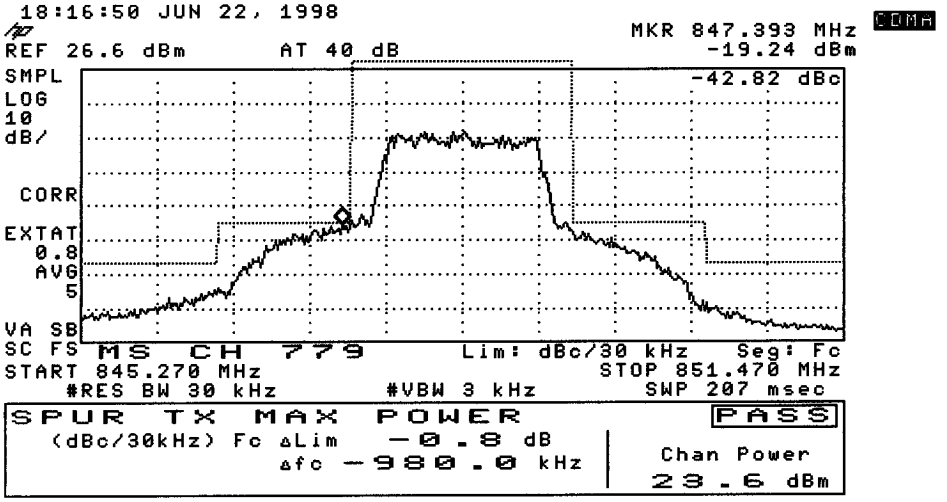


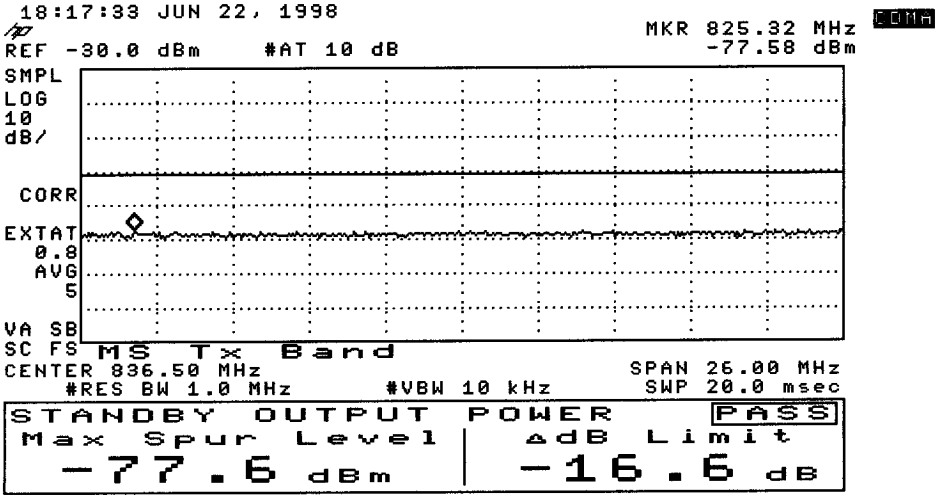
6 ピン・ミニモールド外形図（単位：mm）



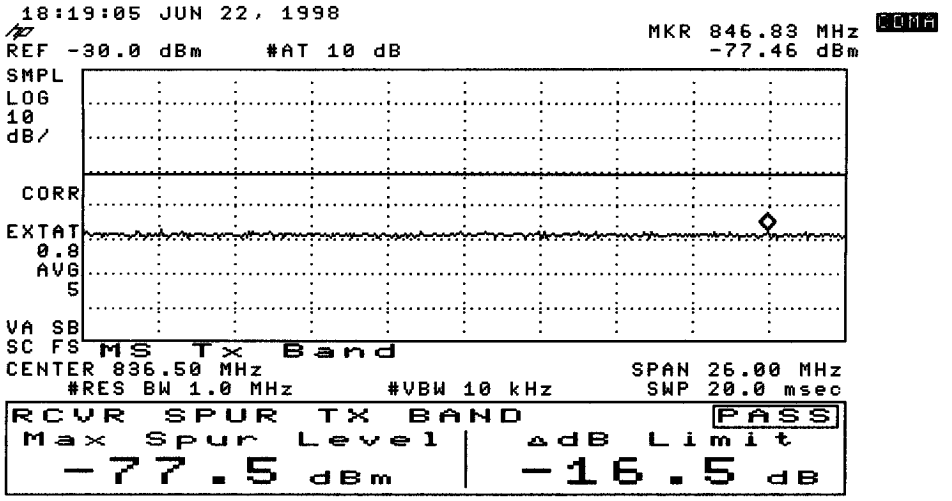
12. Test Reports

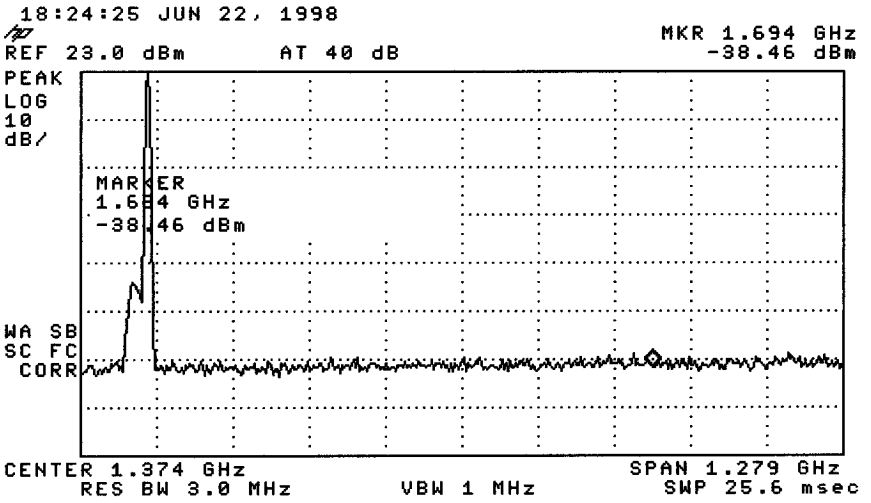

18:14:28 JUN 22, 1998
REF -9.9 dBm
AT 10 dB
MKR 845.922 MHz
-75.01 dBm
-62.07 dBc
SMPL
LOG
10
dB/
CORR
EXTAT
0.8
AVG
5
VA SB
SC FS
MS CH 779
Lim: dBc/30 kHz
Seg: Fc
START 844.770 MHz
STOP 851.970 MHz
#RES BW 30 kHz
#VBW 3 kHz
SWP 240 msec
SPUR CLOSE (Δfc ≤ 25 MHz) [FAST]
PASS
(dBc/30kHz) F- ΔLim
-2.6 dB P
Chan Power
-12.9 dBm


18:16:50 JUN 22, 1998
REF 26.6 dBm
AT 40 dB
MKR 847.393 MHz
-19.24 dBm
-42.82 dBc
SMPL
LOG
10
dB/
CORR
EXTAT
0.8
AVG
5
VA SB
SC FS
MS CH 779
Lim: dBc/30 kHz
Seg: Fc
START 845.270 MHz
STOP 851.470 MHz
#RES BW 30 kHz
#VBW 3 kHz
SWP 207 msec
SPUR TX MAX POWER
PASS
(dBc/30kHz) Fc ΔLim
-0.8 dB
Δfc -980.0 kHz
Chan Power
23.6 dBm

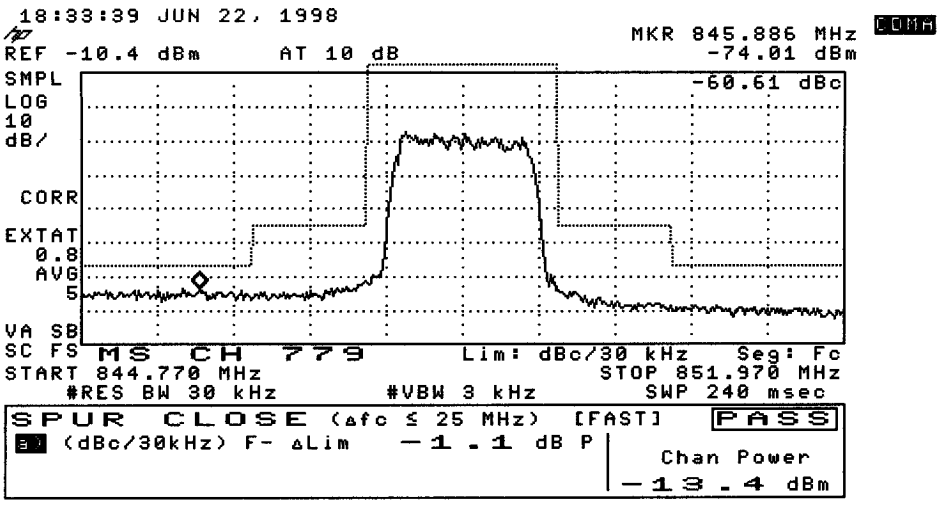

18:17:33 JUN 22, 1998
REF -30.0 dBm
#AT 10 dB
MKR 825.32 MHz
-77.58 dBm
SMPL
LOG
10
dB/
CORR
EXTAT
0.8
AVG
5
VA SB
SC FS
MS Tx Band
CENTER 836.50 MHz
SPAN 26.00 MHz
#RES BW 1.0 MHz
#VBW 10 kHz
SWP 20.0 msec
STANDBY OUTPUT POWER
PASS
Max Spur Level
-77.6 dBm
ΔdB Limit
-16.6 dB

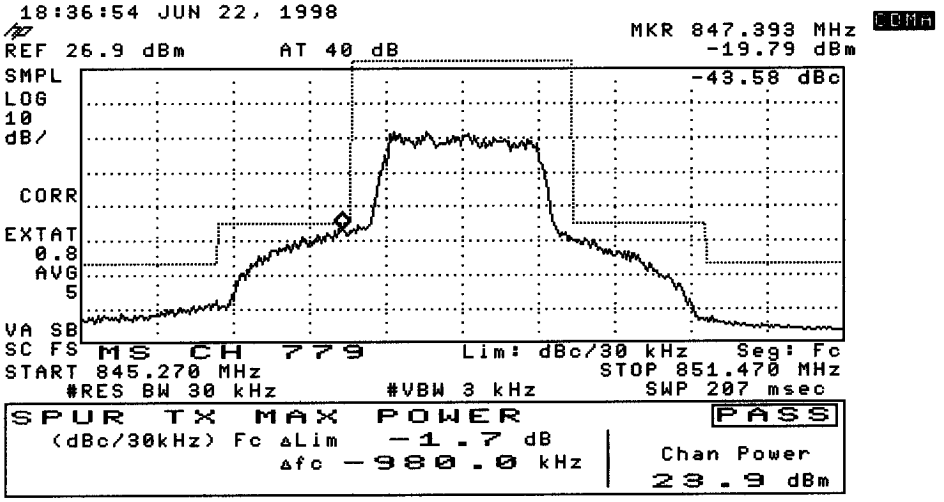
#1

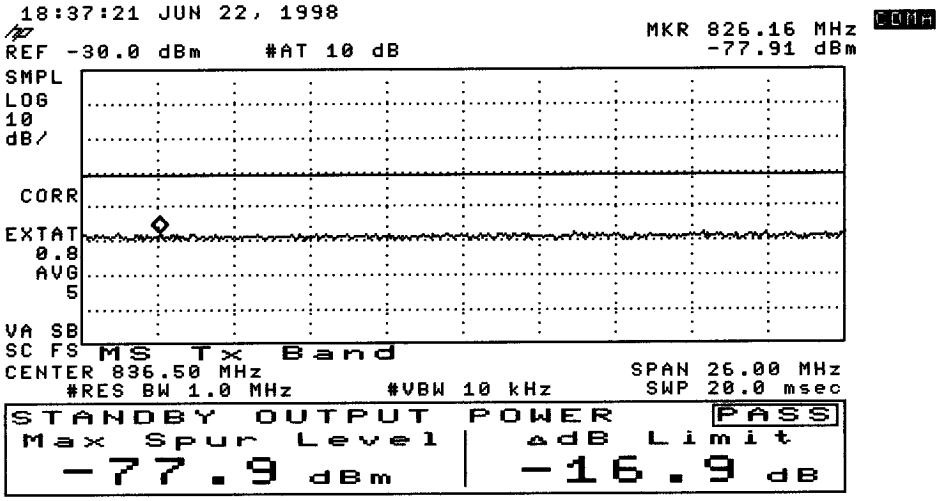

18:19:05 JUN 22, 1998
REF -30.0 dBm
#AT 10 dB
MKR 846.83 MHz
-77.46 dBm
CDMA
SMPL
LOG
10
dB/
CORR
EXTAT
0.8
AVG
5
VA SB
SC FS
MS Tx Band
CENTER 836.50 MHz
#RES BW 1.0 MHz
#VBW 10 kHz
SPAN 26.00 MHz
SWP 20.0 msec
RCVR SPUR TX BAND
PASS
Max Spur Level
-77.5 dBm
ΔdB Limit
-16.5 dB


18:24:25 JUN 22, 1998
REF 23.0 dBm
AT 40 dB
MKR 1.694 GHz
-38.46 dBm
PEAK
LOG
10
dB/
MARKER
1.694 GHz
-38.46 dBm
WA SB
SC FC
CORR
CENTER 1.374 GHz
RES BW 3.0 MHz
VBW 1 MHz
SPAN 1.279 GHz
SWP 25.6 msec

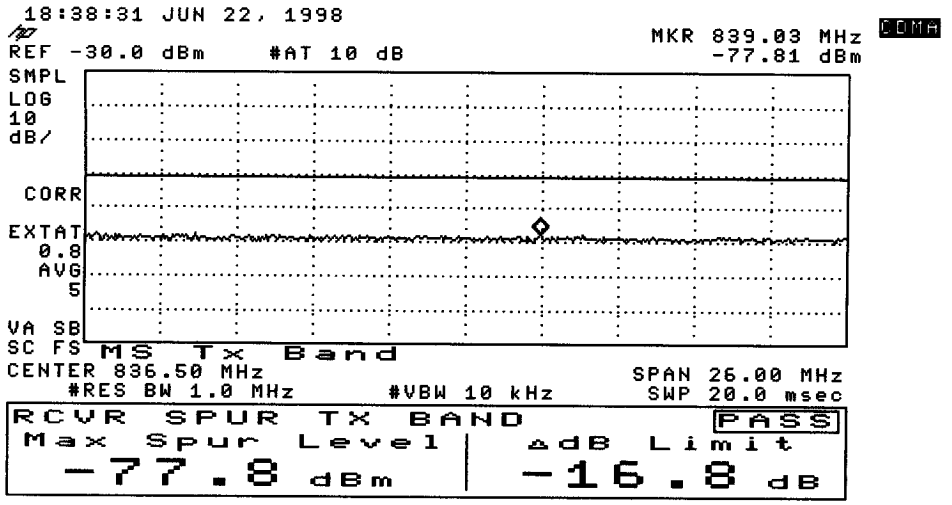
#2

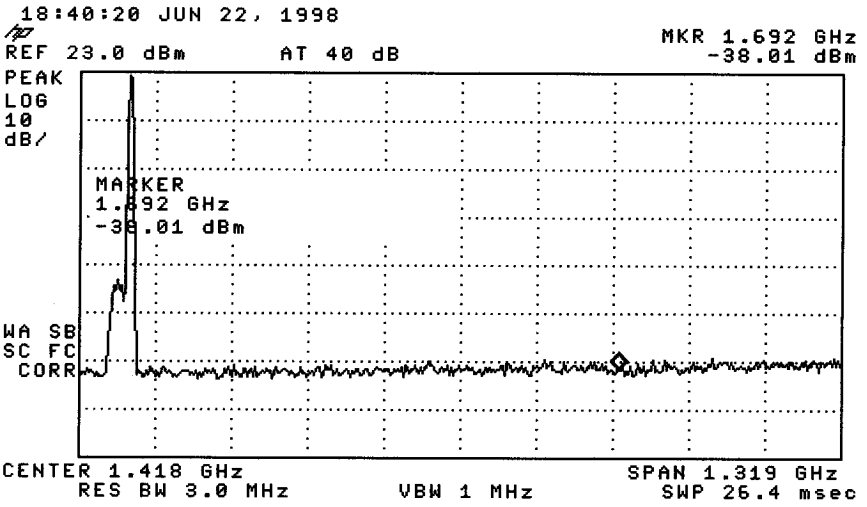

18:33:39 JUN 22, 1998
MKR 845.886 MHz
REF -10.4 dBm
AT 10 dB
-74.01 dBm
SMPL
-60.61 dBc
LOG
10
dB/
CORR
EXTAT
0.8
AVG
5
VA SB
SC FS
MS CH 779
Lim: dBc/30 kHz
Seg: Fc
START 844.770 MHz
STOP 851.970 MHz
#RES BW 30 kHz
#VBW 3 kHz
SWP 240 msec
SPUR CLOSE (Δfc ≤ 25 MHz) [FAST]
PASS
(dBc/30kHz) F- ΔLim
-1.1 dB P
Chan Power
-13.4 dBm


18:36:54 JUN 22, 1998
MKR 847.393 MHz
REF 26.9 dBm
AT 40 dB
-19.79 dBm
SMPL
-43.58 dBc
LOG
10
dB/
CORR
EXTAT
0.8
AVG
5
VA SB
SC FS
MS CH 779
Lim: dBc/30 kHz
Seg: Fc
START 845.270 MHz
STOP 851.470 MHz
#RES BW 30 kHz
#VBW 3 kHz
SWP 207 msec
SPUR TX MAX POWER
PASS
(dBc/30kHz) Fc ΔLim
-1.7 dB
Δfc -980.0 kHz
Chan Power
23.9 dBm


18:37:21 JUN 22, 1998
MKR 826.16 MHz
REF -30.0 dBm
#AT 10 dB
-77.91 dBm
SMPL
LOG
10
dB/
CORR
EXTAT
0.8
AVG
5
VA SB
SC FS
MS Tx Band
CENTER 836.50 MHz
SPAN 26.00 MHz
#RES BW 1.0 MHz
#VBW 10 kHz
SWP 20.0 msec
STANDBY OUTPUT POWER
PASS
Max Spur Level
-77.9 dBm
ΔdB Limit
-16.9 dB

#2


18:38:31 JUN 22, 1998
REF -30.0 dBm
#AT 10 dB
MKR 839.03 MHz
-77.81 dBm
COMA
SMPL
LOG
10
dB/
CORR
EXTAT
0.8
AVG
5
VA SB
SC FS
MS Tx Band
CENTER 836.50 MHz
#RES BW 1.0 MHz
#VBW 10 kHz
SPAN 26.00 MHz
SWP 20.0 msec
RCVR SPUR TX BAND
PASS
Max Spur Level
-77.8 dBm
ΔdB Limit
-16.8 dB


18:40:20 JUN 22, 1998
REF 23.0 dBm
AT 40 dB
MKR 1.692 GHz
-38.01 dBm
PEAK
LOG
10
dB/
MARKER
1.692 GHz
-38.01 dBm
WA SB
SC FC
CORR
CENTER 1.418 GHz
RES BW 3.0 MHz
VBW 1 MHz
SPAN 1.319 GHz
SWP 26.4 msec