OPERATIONAL DESCRIPTION

1. Processor Part

The iXP420 processor is one of the iXP42x series made of Intel. The iXP420 processor controls all functions of OfficeServ SOHO, and an Ethernet MAC controller is equipped with the processor.

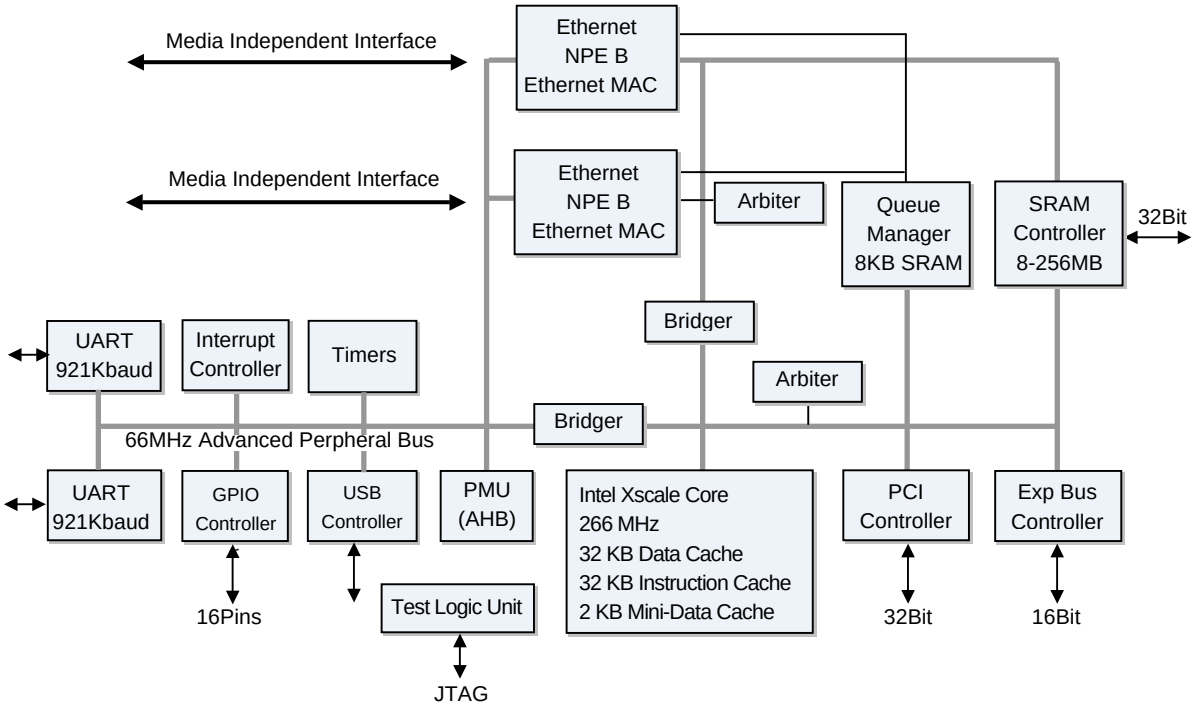


Figure 1. iXP420 Block Diagram

The iXP420 processor is a multi-functional processor. This processor is configured with a 32 bit PCI controller, UARTs, a PC133 SDRAM memory controller, an interrupt controller, a UTOPIA-2, a GPIO, an internal bus of 133 MHz, and Media Independent Interface(MII), and has an Intel Xscale Core architecture.

The main functions of iXP420 are as follows:

- Intel Xscale Core
  - High performance processor is designed based on Xscale Core.
  - 7/8-stage Intel Super-Pipelined RISC Technology.
  - Instruction/data cache of 32 Kbytes
  - Mini data cache of 2 Kbytes
  - Clock rate of 266 MHz
  - ARM Version 5TE Compliant.

- Three Network Processor Engines(NPEs)
  - Ethernet filtering
  - ATM SARing
  - HDLC

- PCI Interface
  - 32 bit interface
  - Generates a clock of 33 MHz, and receives a clock of 0-66 MHz. (A clock can be selected.)
  - Supports the PCI local bus specification, Rev2.2.
  - Up to four external PCIs can be supported using the PCI arbiter.
  - Host/option enabled
  - Master/target enabled
  - Includes two DMA channels.
  - Data of 264 Mbps can be transferred.

- Two MII/RMII Interfaces
  - Supports the 802.3 MII interface and RMII interface.
  - Has an MDIO interface to control two MII/RMII interfaces.

- Two high-speed and serial interfaces
  - Are configured with six signal lines.
  - Can support interfaces of up to 8.192 MHz.
  - Supports a connection to the T1/E1 framers.
  - Supports a connection to Codec/SLIC.
  - Supports eight HDLC channels.

- SDRAM Interface
  - Is configured with 32 bit data and 13 bit address.
  - Supports up to 133 MHz.
  - Maintains up to eight open pages simultaneously.
  - Performs automatic programmable refresh.
  - Delays programmable CAS/data.
  - Supports 8 MB to 256 MB.

- Expansion Interface
  - Is configured with 24 bit address and 16 bit data.
  - Generates eight Chip select signals.
  - Supports interfaces of Intel or Motorola processors.
  - Provides HPI-8/HPI-16 to support DSP of Texas Instrument(TI).

- High Speed UART, Console UART
  - Supports 1200 to 921 Kbaud.
  - Supports Tx/Rx FIFOs of 64 Byte.

- 16 GPIOs
- Four internal timers
- PBGA packages that have 492 pins and can be used at 0~70 °C.

2. Memory Part

Flash ROM(16 MB) and SDRAM(64 MB) are memory components OfficeServ SOHO. A 28F128J3A(flash memory, 16 MB) and two K4S56163Bs(SDRAM, 32 MB and 133 MHz) are in OfficeServ SOHO.

2.1 Flash Memory

The boot area and program image area are not saved in each ROM but are divided into sectors in a single flash memory of OfficeServ SOHO. The IXP420 processor has eight interfaces for expansion. The flash memory is located in '0x00000000' and can be expanded to 16 MB. Also, the flash memory is located in '0x5000_0000' after boot.

The main functions of the flash memory are as follows:

- E28F128J3A 128 Mbit NOR type flash(Intel)
- Is configured with 128 erase blocks of 128 Kbytes. Each block can be erased and be written again up to 100,000 times.
- Block erase time: 0.7 sec
- The flash memory has a buffer of 32 bytes internally, and writes 32 byte data to the buffer. Then, execute a command to enable the state machine to save the buffer in the memory. It takes 12.6 us to write the buffer of 32 byte while it takes about 6.6 sec to write that of 16 Mbytes except for the CPU overload.
- 56 pin TSOP package
- Internal logic power of 3.3 V and I/O logic power of 3.3 V

Flash Host Interface

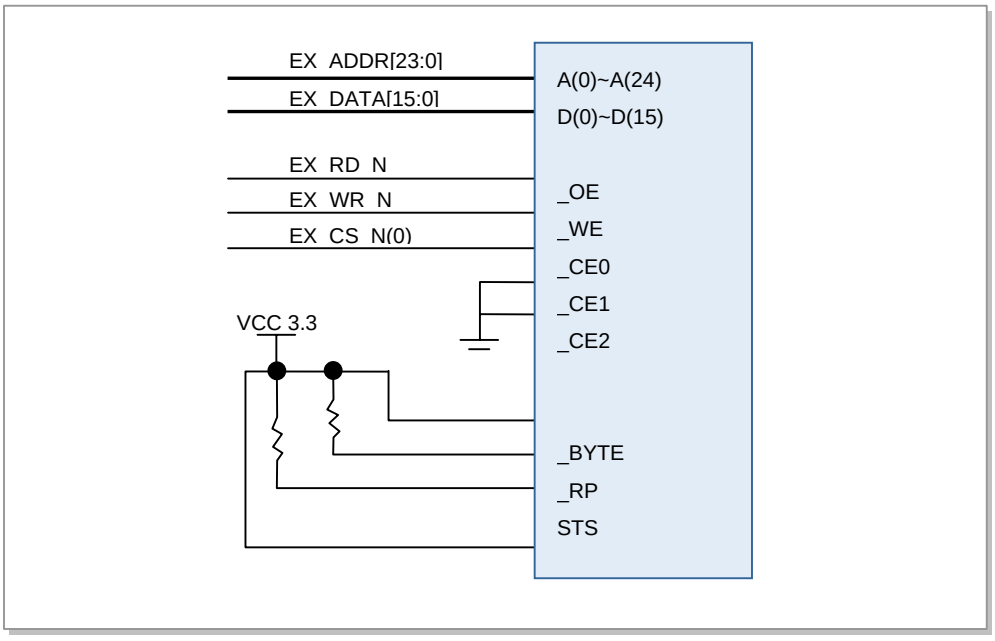


Figure 2. Flash Memory Connection

2.2 Synchronous DRAM (SDRAM)

The main functions of SDRAM are as follows:

- Two K4S561632B(32 Mbytes)-TC60 SDRAMs are used. Total 64 Mbytes
- 15 bit row address and 9 bit column address
- CAS-before-RAS refresh
- 54pin TSOP 400 mil
- Strong ARM accesses SDRAM at a synchronous high data rate.
- Supplies JEDEC standard power of 3.3 V.
- Compatible with LVTTL
- Supports 4 banks.
- MRS cycle through an address key program

1) CAS stop cycle(2 & 3)

2) Bust length(1, 2, 4, 8 & full page)

3) Bust type(Continuity or interrupt)

- Input is performed at both variance of the system clock.
- Reads bust, and reads 1 bit.
- DQM for masking data range
- Automatic refresh
- Refresh cycle of 64ms(Cycle of 4 K)

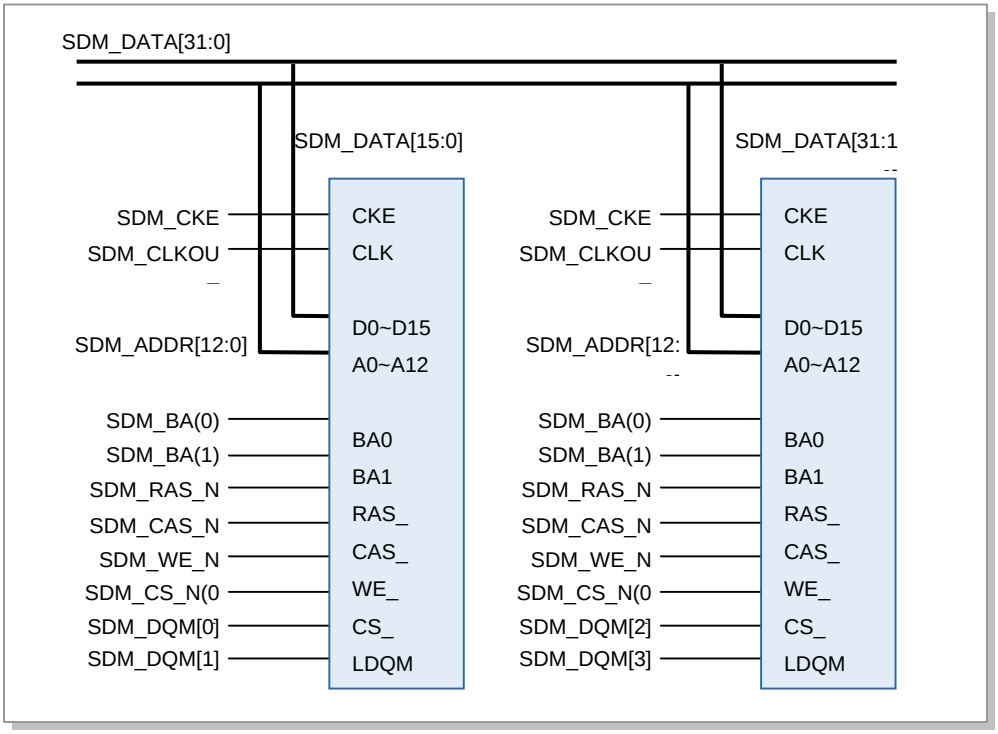


Figure 3. Connections in SDRAM Block

3. WLAN Part

WLAN 802.11g Block

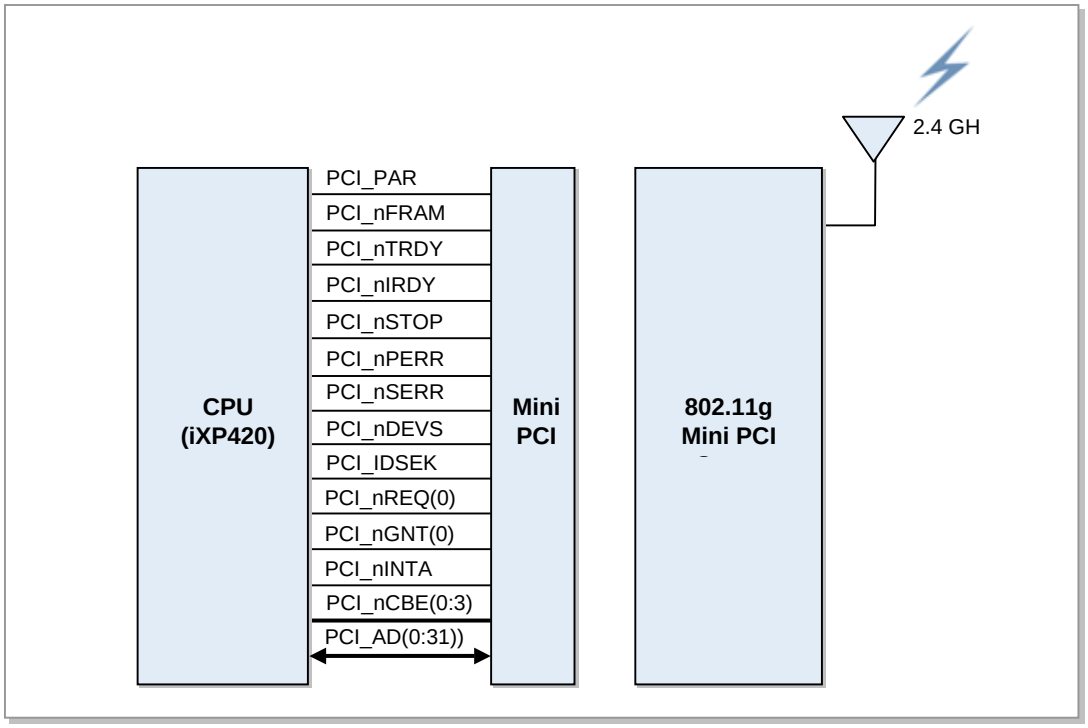
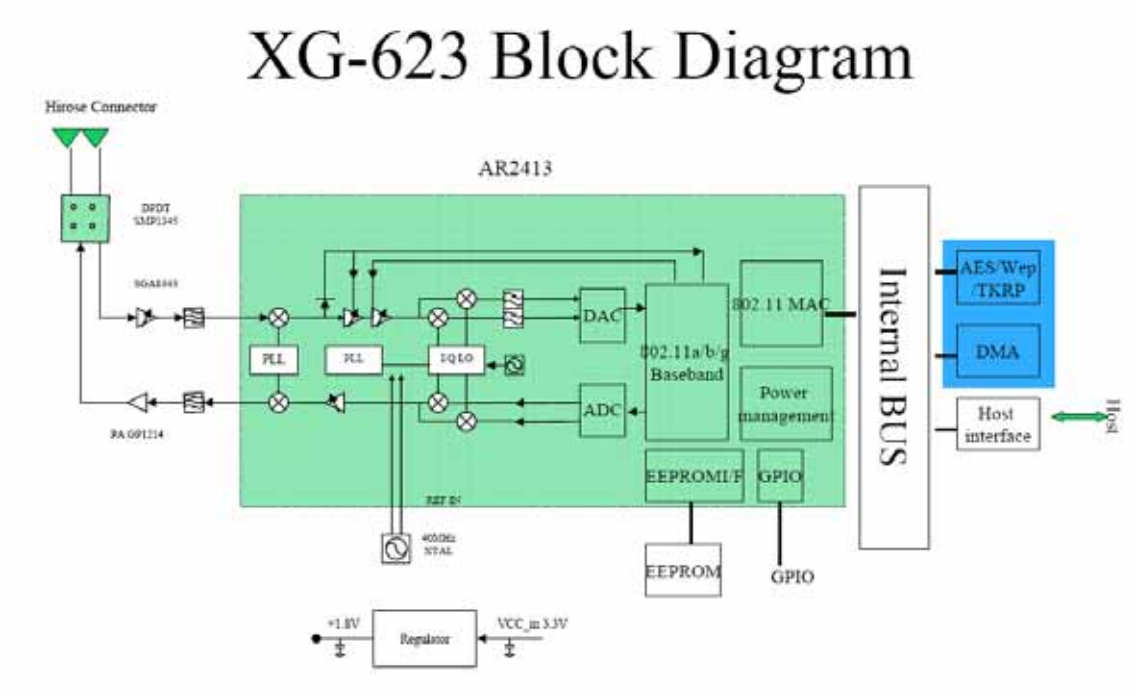


Figure 4.14 WLAN Related Blocks

- Wireless LAN card supports IEEE802.11b/g and its frequency is 2.4 G band. Power used for Tx is below 600 mA, and the card is connected to the host processor through mini-PCI typeⅢB.
- Data communications in the wireless LAN part are made through 802.11 g, and voice communications are made through 802.11b.

4. WLAN Module(XG-623)



XG-623 802.11g/b Compliant Wireless LAN mini PCI Card Specification

4.1. Hardware Specification

1.1 Host Interface:

32-bit Mini PCI Type III -B

1.2 Operating Voltage:

DC 3.3 V ± 5%

1.3 Chipset:

Atheros AR2413 (Single chip)

1.4 Power Consumption:

11g	11b
TX:□550 mA	TX:□550 mA
Rx:□450 mA	Rx:□450 mA

1.5 Radio:

1.5.1 Antenna Connector: 2 U.FL-R-SMT connectors

1.5.2 RF Radiated Power: (± 2 dB)

IEEE802.11g 17dBm (±2dB) @ 54Mbps

17dBm (±2dB) @ 48Mbps

18dBm (±2dB) @ 36Mbps

19dBm (±2dB) @ 6~24 Mbps

IEEE802.11b 19dBm (±2dB) @ 1/2/5.5/11Mbps

1.5.3 Receiver sensitivity with data rate

IEEE 802.11g Sensitivity @ Packet Error Rate□10%

54Mbps:□-65dBm

48Mbps:□-66dBm

36Mbps:□-70dBm

24Mbps:□-74dBm

18Mbps:□-77dBm

12Mbps:□-79dBm

9Mbps:□-81dBm

6Mbps:□-82dBm

IEEE 802.11b Sensitivity @ Packet Error Rate□8%

11Mbps:□-80dBm

5.5Mbps:□-83dBm

2Mbps:□-84dBm

1Mbps:□-87dBm

1.6 Modulation:

IEEE 802.11g (OFDM/DSSS)

48/54 Mbps (QAM-64)

24/36 Mbps (QAM-16)

12/18 Mbps (QPSK)

6/9 Mbps (BPSK)

IEEE 802.11b (DSSS)

5.5/11 Mbps (CCK)

2 Mbps (DQPSK)

1 Mbps (DBPSK)

1.7 Operating Channel:

IEEE 802.11b/g ISM Band

USA (FCC): 2.412GHz ~ 2.462 GHz (CH1 ~ CH11)

Europe (ETSI): 2.412 GHz ~ 2.472 GHz (CH1 ~ CH13)

Japan (TELEC): 11b: 2.412 GHz ~ 2.484 GHz (CH1 ~ CH14)

11g: 2.412 GHz ~ 2.472 GHz (CH1 ~ CH13)

4.2. Software Specification:

1.8 Support OS:

Identical to Atheros Latest Version

1.8.1 Driver: Identical to Atheros Latest Version

1.8.2 Utility: Identical to Atheros Latest Version

1.9 Operation Mode:

1.9.1 Infrastructure mode:

- Seamless roaming within the IEEE802.11b & 11g wireless LAN infrastructure
- Supports WEP encryption

1.9.2 Ad-Hoc mode:

- Peer to peer connection

1.10 Protocol Supported:

TCP/IP

1.11 Security:

RC4 WEP 64(40 bit key) / 128 (104 bit key)/, 152(128 bit key)/ 280(256 bit key)

1.12 Configuration Utility:

1.12.1 Operating System: Windows 98SE/ME/2000/XP

1.12.2 User Selectable Settings: Configuration, AP browser, profile