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DWM3000 Datasheet

Oct. 2002

Open Solution Co., Ltd.

Your Wireless Life!

DWM3000 Datasheet

FEATURES

- Delivers Digital Audio & Data
- Crystal Clear CD Quality Stereo Sound
- 4:1 Audio Compression/Decompression
- Supports 16/24bit Stereo audio data format
- Supports 44.1㎑/48㎑ sampling frequency
- Highly Robust Forward Error Correction
- Modulation Mode:
  - ■ Frequency Hopping Spread Spectrum (FHSS)
  - ■ Adaptive Frequency Selection (AFS)
  - ■ Fixed Channel mode
- TDD (Time Division Duplexing) Mode
- Forward Data Rate: Stereo Audio Data (384Kbps) + Digital Data (16Kbps)
- Reverse Data Rate: Digital Data (28.8Kbps)
- 2.4㎓ Bluetooth RF Chip Interface
- Standard 16-bit 3-wire Stereo Audio Data Interface
- SPI Interface for Non-Audio Data Transmission
- 2.5V Power Supply for Core, 3.3V Power Supply for I/O Interface
- Low Power Consumption : Less than 20㎃
- Power Save Mode
- 48-pin LQFP
- Master/Slave Mode:
  - ■ I2C Master for external booting EEPROM
  - ■ I2C Slave for external MCU Interface
- Broadcasting Mode:
  - ■ Point-to-Point and Point-to-Multi point broadcasting mode selection
  - ■ Master and single slave can communicate bi-directionally in broadcasting mode

OVERVIEW

DWM3000 is a digital audio processor IC encompassing apt-X™ audio compress/decompress algorithm for wireless transmission of crystal-clear CD quality audio data.

For digital transmission the analog audio signals are sampled at 48㎑ and converted to 1.536Mbps digital data through an external 16-bit stereo audio codec. The digitized data are apt-X™ 4:1 compressed to 384Kbps stream data for efficient transmission. Redundancy bits for forward error correction (FEC), synchronization flags, and control signals for time-division duplexing (TDD) are appended to form data frames for error-free transmission.

In the receiver(Slave), synchronization flags and control data are first detected from the input stream. FEC decoder corrects any errors that may have been introduced during the transmission and produces error-free compressed audio data. The compressed audio is decompressed into 16-bit stereo PCM audio data through digital signal processing blocks. External audio codec converts the PCM data to 2-channel (left and right) analog audio signals.

The Tx/Rx controller is in charge of several functions such as radio channel setup, frequency hopping for interference reduction and generation of control signal for TDD and external RF chip.

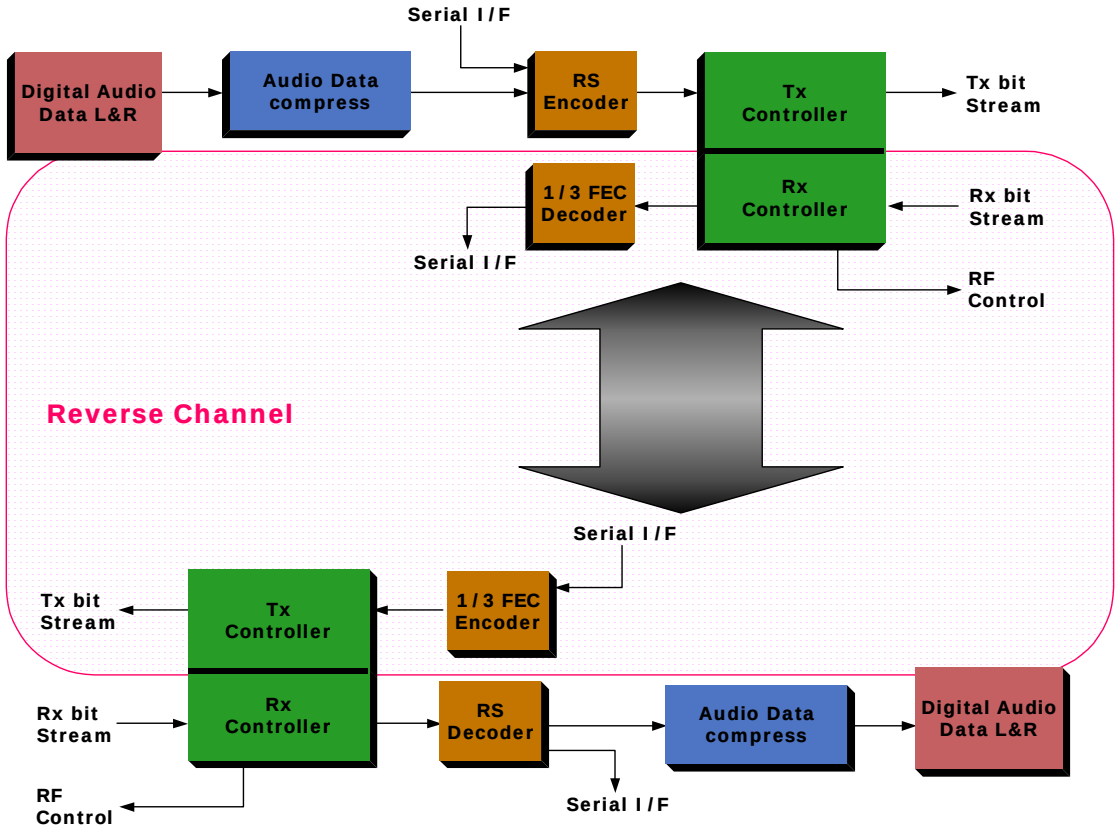
In audio mode, the transmitter(Master) can send additional 16Kbps digital data simultaneously with stereo audio data. Full digital data communication of 400Kbps is also available in data mode where audio codec and compression/decompression block are bypassed. The receiver(Slave) supports 28.8Kbps reverse digital data communication that can be used for transmitter(Master) control or other applications.

APPLICATION

Wireless Headphone
Wireless Headset
Wireless Speaker/Microphone
Wireless Keyboard/Mouse
Wireless System control
Short Distance Data Link
Smart Toy

OPERATIONAL BLOCK DIAGRAM

Figure 1. DWM3000 Functional Block Diagram



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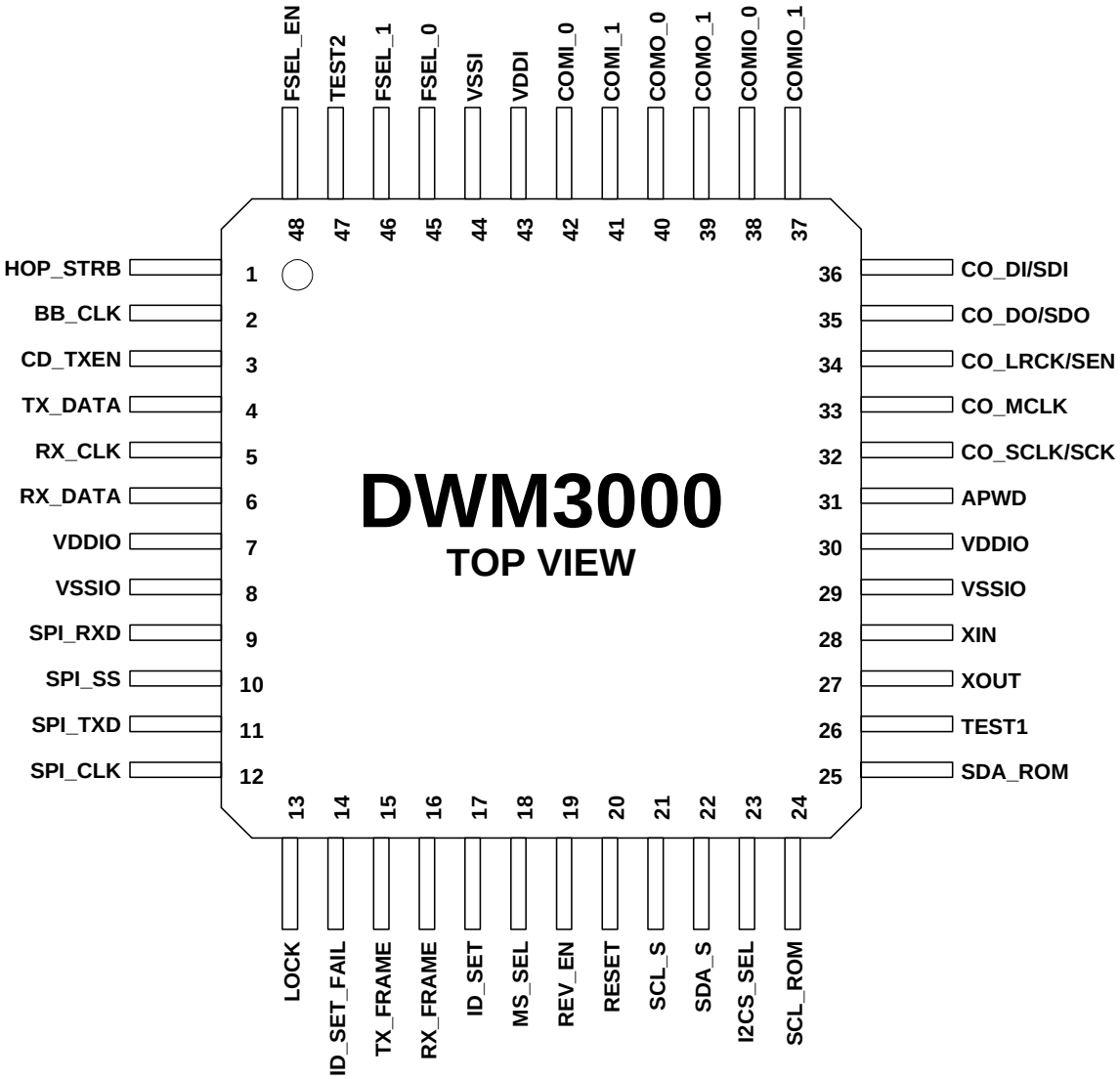
This section describes 48 pins of DWM3000. Pins are grouped in Power, RESET/XIN-XOUT, Radio Interface, I2C Master/Slave, Audio Codec Interface/SPI, and Baseband.

1.1 Pin Diagram

Figure 2. DWM3000 Pin Diagram



1.2 Pin Description (Sort by PIN Number)

Signal Type Definition

- DI: Input pin
- DO: Output pin
- DIO: In/Out Bi-directional pin
- DP: Power pin
- DG: Ground pin

Table 1. Pin Description (Sort by PIN Number)

PIN Number	PIN NAME	I/O	DESCRIPTION
1	HOP_STRB	DO	SiW1502 I/F signal reserved for Hopping strobe
2	BB_CLK	DI	SiW1502 I/F signal reserved for 16㎒ clock input
3	CD_TXEN	DIO	SiW1502 I/F signal reserved for Tx enable out and Rx carrier detect in (Normally pulled down pad)
4	TX_DATA	DO	SiW1502 I/F signal reserved for Tx data stream
5	RX_CLK	DI	SiW1502 I/F signal reserved for 1㎒ reference clock
6	RX_DATA	DI	SiW1502 I/F signal reserved for Rx data stream
7, 30	VDDIO	DP	Digital I/O pad power = 3.3V
8, 29	VSSIO	DG	Digital I/O pad ground
9	SPI_RXD	DO	SiW1502 I/F signal reserved for SPI data to RF module
10	SPI_SS	DO	SiW1502 I/F signal reserved for SPI enable to RF module
11	SPI_TXD	DI	SiW1502 I/F signal reserved for SPI data from RF module
12	SPI_CLK	DO	SiW1502 I/F signal reserved for SPI clock to RF module
13	LOCK	DO	Demodulator sync detection signal
14	ID_SET_FAIL	DO	Indicate ID set success or fail, “1”= Fail
15	TX_FRAME	DO	Tx Frame sync signal
16	RX_FRAME	DO	Rx Frame sync signal
17	ID_SET	DI	Device ID set mode, “1”= Active
18	MS_SEL	DI	Master("1")/Slave("0") mode selection
19	REV_EN	DI	P2P("1")/Broadcasting("0") mode select
20	RESET	DI	Active Low system reset
21	SCL_S	DI	3-wire Interface Slave clock input pin reserved for MCU interface
22	SDA_S	DIO	3-wire Interface Slave data pin reserved for MCU Interface
23	I2CS_SEL	DI	Reserved pin to select LSB of 3-wire audio interface address of DWM3000, “0”= 1010110, or “1”= 1010111

PIN Number	PIN NAME	I/O	DESCRIPTION
24	**SCL_ROM**	**DO**	I2C master clock output pin reserved for EEPROM access
25	**SDA_ROM**	**DIO**	I2C master data pin reserved for EEPROM access I2C address of EEPROM is reserved for 1010001
26	**TEST1**	**DI**	Set to “0” in normal operation
27	**XOUT**	**DO**	12.288㎒ crystal output
28	**XIN**	**DI**	12.288㎒ crystal input
31	**APWD**	**DO**	Reserved for External Audio ADC power down control, “0”= Power down
32	**CO_SCLK/SCK**	**DIO**	1.536㎒/3.072㎒ Audio serial clock/SPI clock/1㎒ SPI clock
33	**CO_MCLK**	**DIO**	12.288㎒ Audio master clock
34	**CO_LRCK/SEN**	**DIO**	48㎑ Audio sampling clock/SPI Enable signal
35	**CO_DO/SDO**	**DO**	Audio data output stream/SPI data output stream
36	**CO_DI/SDI**	**DI**	Audio data input stream/SPI data input stream
37	**COMIO_1**	**DIO**	Remote control command inout
38	**COMIO_0**	**DIO**	Remote control command inout
39	**COMO_1**	**DO**	Remote control command output
40	**COMO_0**	**DO**	Remote control command output
41	**COMI_1**	**DI**	Remote control command input
42	**COMI_0**	**DI**	Remote control command input
43	**VDDI**	**DP**	Digital Core block power = 2.5V
44	**VSSI**	**DG**	Digital Core block ground
45	**FSEL_0**	**DI**	LSB of RF frequency selection
46	**FSEL_1**	**DI**	MSB of RF frequency selection
47	**TEST2**	**DI**	Set to “1” in normal operation
48	**FSEL_EN**	**DI**	Enable external RF frequency selection, “1”= Enable

Table 2. External Frequency Selection Table

FSEL_EN	FSEL_1	FSEL_0	Frequency Level
1	0	0	2,410㎒
1	0	1	2,430㎒
1	1	0	2,450㎒
1	1	1	2,470㎒
0	X	X	Use External EEPROM or MCU Setting

1.3 Pin Description (Sort by Functions)

Signal Type Definition

- DI: Input pin
- DO: Output pin
- DIO: In/Out Bi-directional pin
- DP: Power pin
- DG: Ground pin

Table 3. Pin Description (Sort by Functions)

PIN Type	PIN Function	Resources
Power	Digital Core block & I/O Power	Table 4. Power Pin Description
RESET/XIN-XOUT	RESET/Crystal associated Pins	Table 5. RESET/XIN-XOUT Pin Description Figure 3. DWM3000 Crystal Connection Circuit
Radio Interface	Silicon Wave's Bluetooth RF (SiW1502) Interface Pins	Table 6. Radio Interface Pin Description Figure 4. Connection between DWM3000 and SiW1502
I2C Master	EEPROM Interface	Table 7. I2C Master Pin Description Figure 5. EEPROM Current Address Read Operation Figure 6. EEPROM Random Address Read Operation Figure 7. EEPROM Sequential Read Operation Figure 8. EEPROM Byte Write Operation Figure 9. EEPROM Page Write Operation
I2C Slave	MCU Interface	Table 8. I2C Slave Pin Description Figure 11. Register Read Operation Figure 12. Register Write Operation Figure 13. Tx Data Buffer Write Operation Figure 14. Rx Data Buffer Read Operation
Audio CODEC Interface/SPI	Audio CODEC Interface for audio data/SPI for stream data	Table 9. Audio CODEC Interface/SPI Pin Description Table 10. DWM3000 Audio Serial Clock Figure 15. Audio Data Interface Timing Diagram Figure 16. Master Mode SPI Timing Diagram Figure 17. Slave Mode SPI Timing Diagram
Baseband	Operation Mode Control, Internal Status of Chip, Pin-to-Pin Direct Transmission	Table 11. Baseband Pin Description Table 12. COMI, COMO, COMIO Pin Mapping

1.3.1 Power Pins

Table 4. Power Pin Description

PIN NAME	PIN Number	I/O	DESCRIPTION
VDDI	**43**	**DP**	Digital Core block power = 2.5V
VSSI	**44**	**DG**	Digital I/O pad ground
VDDIO	**7, 30**	**DP**	Digital I/O pad power = 3.3V
VSSIO	**8, 29**	**DG**	Digital I/O pad ground

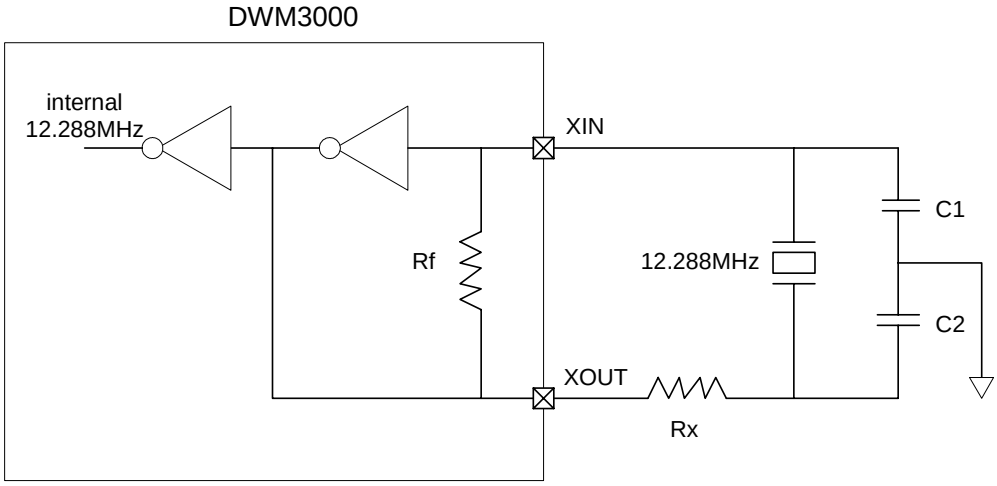
1.3.2 RESET/XIN-XOUT Pins

XIN/XOUT are crystal associated pins. These are oscillator pad for master clock of audio part. These are connected to an external 12.288MHz crystal. The audio master clock is an internal actual signal and set by parameter registers. DWM3000 chooses between 12.288MHz clock through XIN/XOUT pad and 12.288MHz CO_MCLK (Refer to Table 9. Audio CODEC Interface/SPI Pin Description). Figure 3 shows connection circuit between DWM3000 and crystal.

Table 5. RESET/XIN-XOUT Pin Description

PIN NAME	PIN Number	I/O	DESCRIPTION
RESET	**20**	**DI**	Active low system reset derived from external Power On Reset Circuit When RESET signal is active, all registers are initialized (1 or 0). After power on, this signal should maintain low state at least 1ms, and then it is in high state. The holding time (1ms) is for SiW1502 RF chip to set BB_CLK which is a baseband clock. If RESET is released and BB_CLK is input, DWM3000 starts its operation.
XIN	**28**	**DI**	This is an input pin to an oscillator. [Opposite polarity to XOUT]
XOUT	**27**	**DO**	This is an output pin to an oscillator. When it is used for internal audio clock, it has the same polarity as XIN by inverting an output of oscillator.

Figure 3. DWM3000 Crystal Connection Circuit



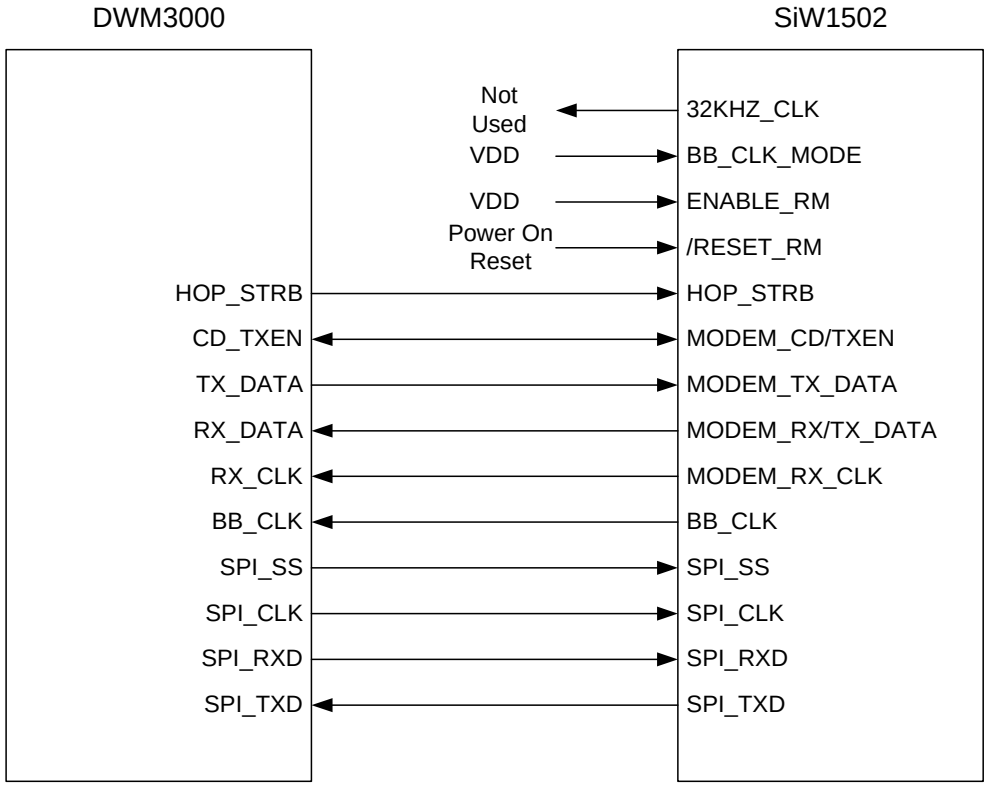
1.3.3 Radio Interface Pins

All signals in Radio Interface block are designed to interface to SiW1502 directly. In addition, BB_CLK is connected to Clock Generation block to create clock. Figure 4 shows connection between DWM3000 and RF Chip SiW1502.

Table 6. Radio Interface Pin Description

PIN NAME	PIN Number	I/O	DESCRIPTION
TX_DATA	**4**	**DO**	This is a 1MHz symbol data stream sent to SiW1502. It is connected to 'MODEM_TX_DATA' of SiW1502.
RX_DATA	**6**	**DI**	This is a 1MHz symbol data stream sent to DWM3000. It is connected to 'MODEM_RX/TX_DATA' of SiW1502.
RX_CLK	**5**	**DI**	This is a 1MHz symbol clock generated from SiW15002. RX_DATA received from SiW1502 is synchronized to rising edge of RX_CLK. It is connected to 'MODEM_RX_CLK' of SiW1502.
CD_TXEN	**3**	**DIO**	This is a bi-directional pin connected to 'MODEM_CD/TXEN' of SiW1502. If it is used for an input signal, it detects a carrier generated by SiW1502 in receive mode. If it is used for an output signal, it enables TX signal in transmit mode.
HOP_STRB	**1**	**DO**	This is in high state in the range of data transmit/receive and its before and behind interval where data are ready for transmit/receive. It is connected to 'HOP_STRB' of SiW1502. Its timing accords with requirement of SiW1502.
BB_CLK	**2**	**DI**	SiW1502 can generate 8/16/32MHz BB_CLK according to operation condition, but DWM3000 uses only 16MHz BB_CLK. 'BB_CLK_MODE' pin in SiW1502 preserves high state. It is connected to 'BB_CLK' of SiW1502.
SPI_TXD	**11**	**DI**	This is a receive signal of RSSI value and etc (no transmit/receive stream data). It is connected to 'SPI_TXD' of SiW1502.
SPI_CLK	**12**	**DO**	DWM3000 dispenses 16MHz clock and outputs 4MHz clock. 'SPI_TXD' and 'SPI_RXD' are synchronized to rising edge of 'SPI_CLK'. DWM3000 does not generate SPI_CLK during high 'SPI_SS'. It is connected to 'SPI_CLK' of SiW1502. Its timing accords with requirement of SiW1502.
SPI_SS	**10**	**DO**	SPI_RXD and SPI_TXD are valid only when SPI_SS is low. When SPI_SS is high, SPI_CLK preserves low state and does not generate clock signal. It is connected to 'SPI_SS' of SiW1502. Its timing accords with requirement of SiW1502.
SPI_RXD	**9**	**DO**	This is command information (no transmit/receive stream data) sent to SiW1502. It is connected to 'SPI_RXD' of SiW1502.

Figure 4. Connection between DWM3000 and SiW1502



For more details, refer to ‘SiW1502 Radio Modem IC Interface and Programming Guide (Nov. 9. 2001, Silicon Wave)’ and ‘SiW1502 Radio Modem Technical Specification (Jul. 16. 2001, Silicon Wave)’.

1.3.4 I2C Master Pins

After DWM3000 is on, it loads operation parameters from EERPOM using I2C master. DWM3000 interfaces to 128x8b or 256x8b EEPROM. EEPROM's I2C slave address is fixed to '1010001'. Functional timing of EEPROM Interface accords with 'AT24C21 2-wire serial EEPROM datasheet' from ATMEL.

Table 7. I2C Master Pin Description

PIN NAME	PIN Number	I/O	DESCRIPTION
SDA_ROM	**25**	**DIO**	This is an I2C data signal to access to an external EEPROM through I2C master within DWM3000. It assumes that a pull-up register is connected.
SCL_ROM	**24**	**DO**	This is an I2C clock signal to access to an external EEPROM through I2C master within in DWM3000. It assumes that a pull-up register is connected. [Typical frequency is 100KHz.]

1.3.4.1 EEPROM Read Operation

EEPROM read operation is used for boot procedure. It has three modes, Current Address Read Mode, Random Address Read Mode, and Sequential Read Mode. Current Address Read Mode loads data of current address where EEPROM's address counter points. Random Address Read Mode loads data within EEPROM's address where it is desired. Sequential Read Mode loads in serial order data of address where EEPROM's address counter points or set by Random Address Read Mode by one increment. This procedure continues till stop command is transmitted.

In boot procedure, DWM3000 reads 00H ~ 5CH address of data in order using Sequential Read Mode and loads them into internal parameter registers.

Figure 5. EEPROM Current Address Read Operation

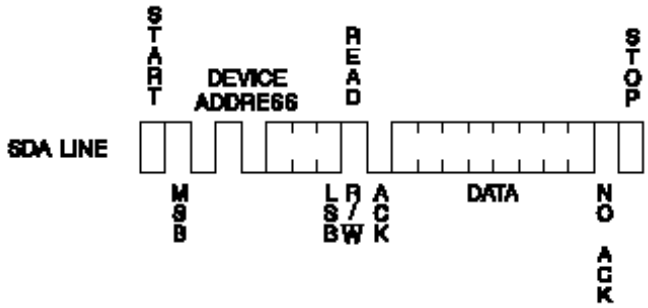


Figure 6. EEPROM Random Address Read Operation

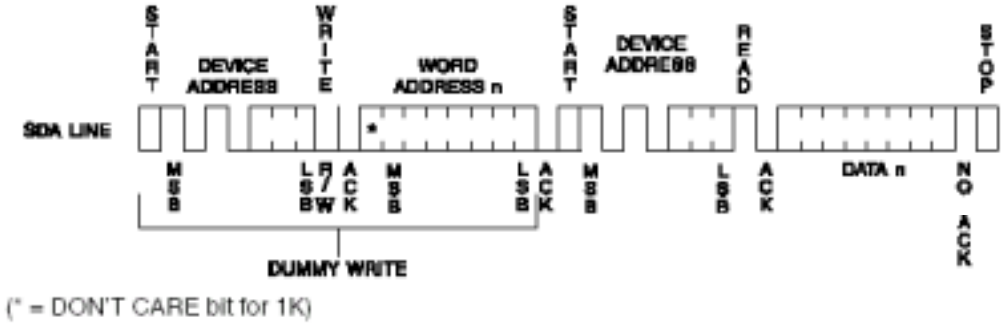
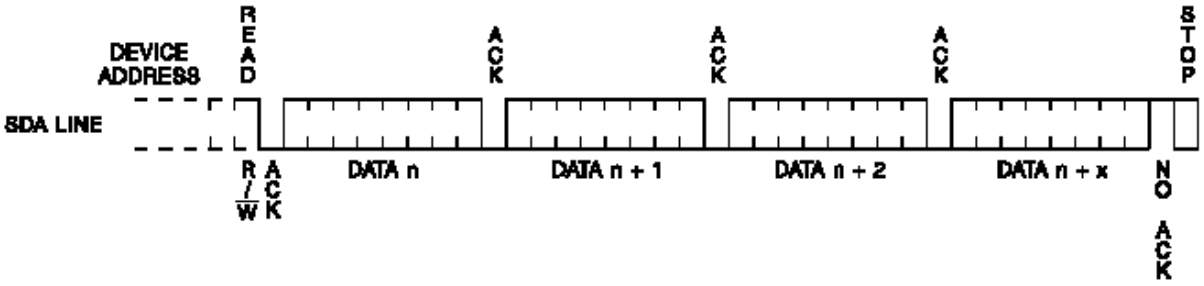


Figure 7. EEPROM Sequential Read Operation



1.3.4.2 EEPROM Write Operation

EEPROM write operation is used for Device ID storage. It has two modes, Byte Write Mode and Page Write Mode. Byte Write Mode stores data into one address of EEPROM. Page Write Mode stores sequentially data into specific address of EEPROM by an increment till stop command is transmitted.

In DWM3000's Device ID save procedure, DWM3000 writes Master Device ID into EEPROM's 04H ~ 07H address using Page Write Mode.

Figure 8. EEPROM Byte Write Operation

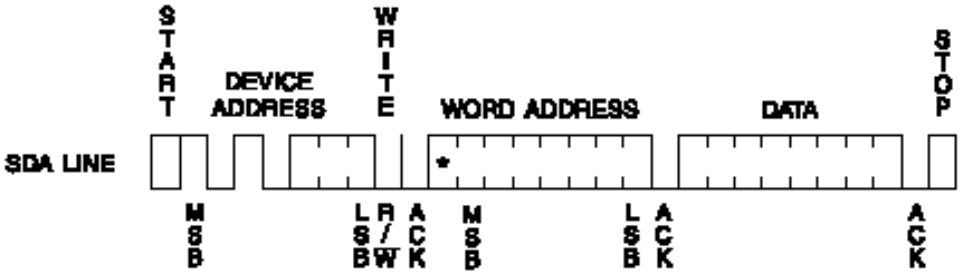
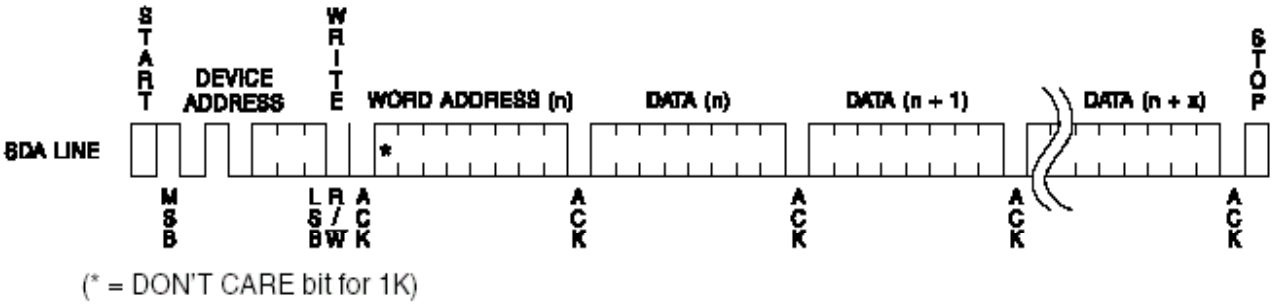


Figure 9. EEPROM Page Write Operation



(* = DON'T CARE bit for 1K)

1.3.4.3 I2C Master Bus Timing

Refer to I2C bus specification.

1.3.5 I2C Slave Pins

DWM3000 interfaces to I2C master MCU using I2C slave in the following case:

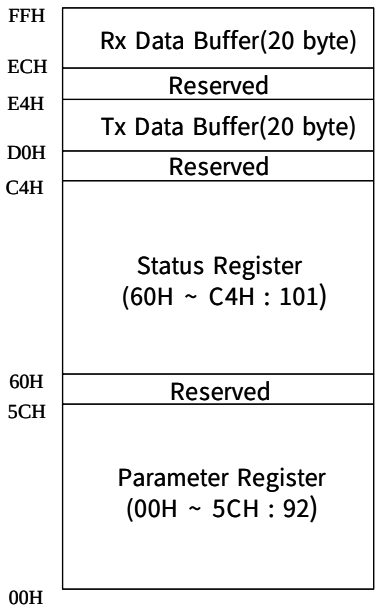
- No EEPROM
- Access to parameter or status registers in DWM3000 during operation
- Write/Read data into/from Tx/Rx Data Buffer
- Additional transmit/receive data except audio data
  - ■ Master → Slave (16Kbps)
  - ■ Slave → Master (28.8Kbps)

Table 8. I2C Slave Pin Description

PIN NAME	PIN Number	I/O	DESCRIPTION
I2CS_SEL	**23**	**DI**	This is to select I2C slave's address to interface to MCU. [I2CS_SEL=0]: Slave address is '1010110' [I2CS_SEL=1]: Slave address is '1010111' As it uses pull-down pad, it is set to '1010110' by default.
SDA_S	**22**	**DIO**	This is an I2C data signal to access to an external MCU through I2C slave in DWM3000. It assumes that a pull-up register is connected.
SCL_S	**21**	**DI**	This is an I2C clock signal to access to an external MCU through I2C slave in DWM3000. It receives I2C clock generated from MCU.

DWM3000 includes transmit/receive buffer for asynchronous data transmit/receive. DWM3000's register/buffer map is shown in Figure 10. An address is comprised of 8 bits.

Figure 10. DWM3000 Address Map



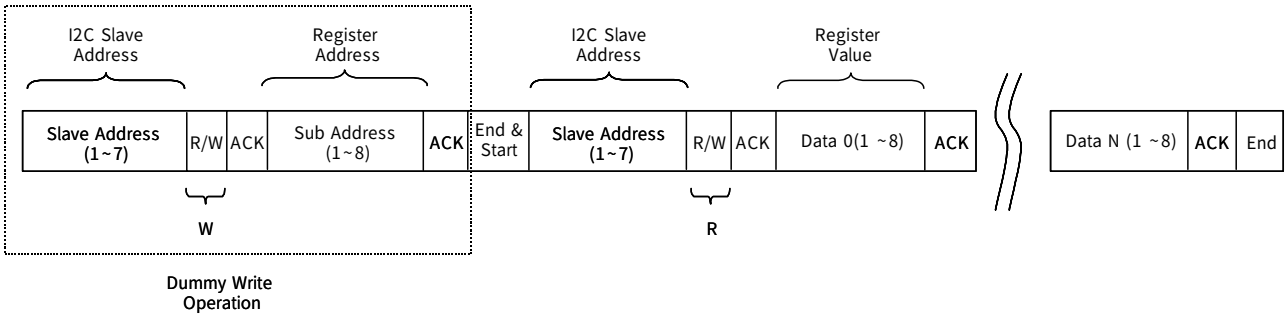
1.3.5.1 Register Read/Write Operation

External MCU (I2C master) can read/write data from/into registers in DWM3000 through I2C slave. In case of no EEPROM, it can perform booting procedure by writing data into parameter registers. In addition, it can check the operation status of DWM3000 by reading data from status registers.

1.3.5.1.1 Register Read Operation

External MCU can load data from all registers within DWM3000. Figure 11 shows how external MCU reads data from a specific register or register group.

Figure 11. Register Read Operation

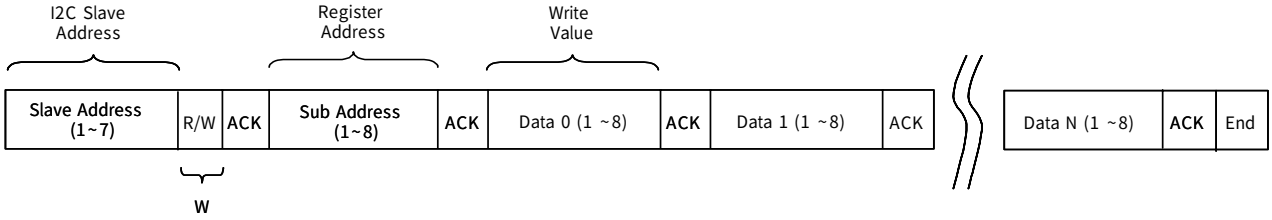


To read data in specific register, start address of the register or register group to be read should be appointed via dummy write operation. Register's data is read from the designated register sequentially by address increment till End signal is transmitted.

1.3.5.1.2 Register Write Operation

External MCU can write data into parameter registers in DWM3000 through I2C slave. Figure 12 shows how external MCU writes data into a specific register.

Figure 12. Register Write Operation



To write data into specific registers or register group, the procedure is as follows:

1. Transmit I2C slave address in write mode
2. Designate specific register by transmitting address of register to write
3. Transmit data (8-bit) to write

Write operation is done sequentially from designated start address till End signal is shown.

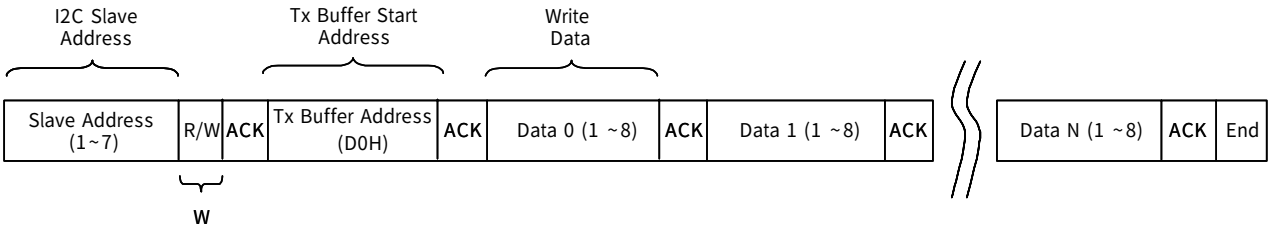
1.3.5.2 Tx/Rx Data Buffer Operation

External MCU can write data to be sent into transmit buffer or read received data from receive buffer through DWM3000's I2C slave. The buffer is implemented with FIFO. As the buffer encompasses address counter, they don't have to points out the specific address of buffer. However, in I2C slave interface, to distinguish I2C slave interface from register map interface, transmit/receive buffer 's start address is always assigned to D0H/ECH (That is, Tx Buffer' start address: D0H, Rx Buffer's start address: ECH).

1.3.5.2.1 Tx Data Buffer Write Operation

Write operation of Tx Data Buffer using I2C slave is basically identical to write operation of register. The difference between those is that sub-address is designated to Tx Buffer's start address (D0H). Tx Data Buffer allows only write operation for external devices. Figure 13 shows how external MCU writes data into Tx Data Buffer.

Figure 13. Tx Data Buffer Write Operation



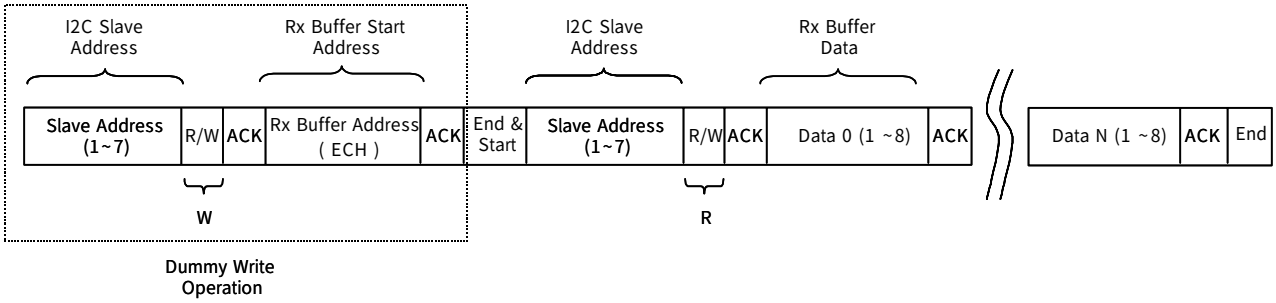
As Tx Data Buffer is formed of FIFO, buffer itself does not have its address. To differ from register map interface, Tx Buffer Start Address (D0H) should be always transmitted after sending I2C slave address. Length of transmit data is determined by space of Tx Buffer. Transmit data can be sent up to 20 Bytes in case Tx Data Buffer is empty.

When data is transmitted via Tx Data Buffer, Tx Data Buffer's status flags (0x89, 0x8A) in Status Registers should be checked. Then, data should be sent as long as buffer is available not to overwrite data to transmit.

1.3.5.2.2 Rx Data Buffer Read Operation

Read operation of Rx Data Buffer using I2C slave is basically identical to read operation of register. The difference between those is that sub-address is designated to Rx Buffer's start address (ECH). Rx Data Buffer allows only read operation for external devices. Figure 14 shows how external MCU reads data from Rx Data Buffer.

Figure 14. Rx Data Buffer Read Operation



As Rx Data Buffer is formed of FIFO, they don't have to assign a specific address for buffer read. To differ from register map or Tx Data Buffer interface, Rx Buffer Start Address (ECH) should be appointed. MCU can read received data from Rx Data Buffer. The length of read data can be checked via status register (0x89, 0x8C)

1.3.5.3 I2C Slave pin timing

Refer to I2C bus specification.

1.3.6 Audio CODEC Interface/SPI Pins

To transmit/receive audio data, DWM3000 adopts general 3-wire audio data interface. It consists of audio serial clock, audio sampling clock, audio serial data input(or output). When DWM3000 transmits/receives stream data instead of audio data, SPI is adopted. That is, it is comprised of serial clock, serial data enable, serial data input(or output) and each is used by sharing audio data interface pin.

Table 9. Audio CODEC Interface/SPI Pin Description

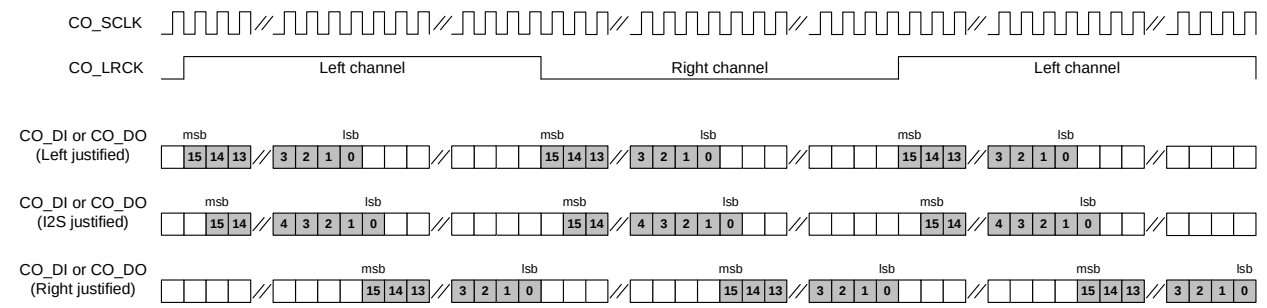
PIN NAME	PIN Number	I/O	DESCRIPTION
CO_MCLK	**33**	**DIO**	12.288MHz audio master clock This can be defined as input or output depending on applications. [AMCLK_SEL=1 or MS_SEL=0(Slave Mode)]: CO_MCLK is output. The other is CO_MCLK is input. When it is output, its source is signal derived from XIN/XOUT pad. In SPI mode, it is not necessary.
CO_SCLK/ SCK	**32**	**DIO**	1.536㎒/3.072㎒ Audio serial clock/SPI clock/1㎒ SPI clock This is used for audio data application or stream data application. In audio data application mode, it is serial clock of audio data. In stream data application mode, it is serial clock of stream data. When DWM3000 is used for audio application and master system transmitting audio data, this pin is bi-directional clock. When DWM3000 is used for slave system receiving audio data, it is an output. Table 10 shows Audio Serial Clock Frequency when it is used for audio data application. When DWM3000 is used for stream data application and master system transmitting stream data, this pin is bi-directional clock. When DWM3000 is used for slave system receiving stream data, it is an output. Serial clock per frame is 960-clock. [Frame produces per 2.5ms. Stream data can be transmitted by 120B per frame. Consequently, serial clock is 120x8 per frame.] In case it is an output, SPI stream data clock produces by 1MHz. In case it is an input, the range of 500KHz~1MHz frequency is valid.
CO_LRCK/SEN	**34**	**DIO**	When audio application, it is used for 48KHz or 44.1KHz symbol clock of audio data. When stream data application, it is used for SPI serial data enable. It divides serial data into a byte. In addition, it can be input or output according to applications.
CO_DI/SDI	**36**	**DI**	When audio application, it is used for serial data input of audio data. The audio serial data changes at a falling edge of ‘CO_SCLK/SCK’. When stream data application, it is used for SPI serial data input. The stream data changes at a rising edge of ‘CO_SCLK/SCK’.
CO_DO/SDO	**35**	**DO**	When audio application, it is used for serial data output of audio data. The audio serial data changes at a falling edge of ‘CO_SCLK/SCK’. When stream data application, it is used for SPI serial data output. The stream data changes at a rising edge of ‘CO_SCLK/SCK’.
APWD	**31**	**DO**	This controls ‘Power Down’ of external Audio CODEC. When it is low state, the external Audio CODEC becomes ‘power down’ state. Before completing initialization by reading parameter register of EEPROM or MCU, it generates ‘power down enable’ signal. ADC_PWDN, DAC_PWDN parameter in register can enable/disable ‘power down’

Table 10. DWM3000 Audio Serial Clock

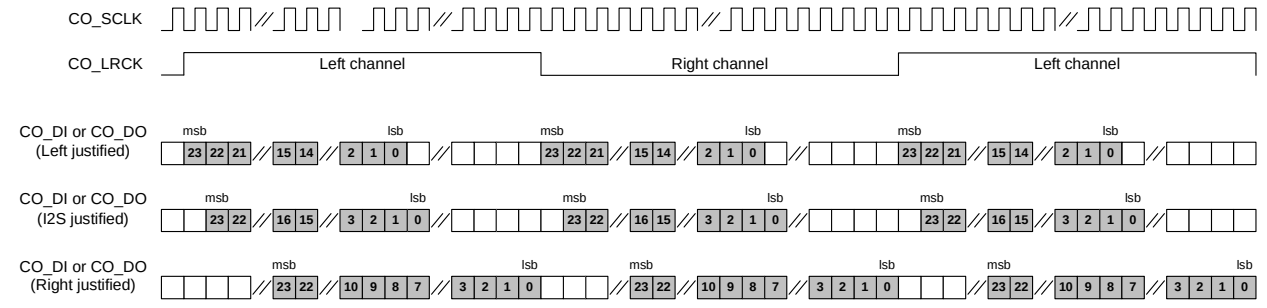
Master/Slave mode	I/O	Frequency (MHz)	Description
Master	I	1.4112	44.1kHz audio sampling(fs)'s 32fs
		2.8224	44.1kHz audio sampling(fs)'s 64fs
		1.536	48kHz audio sampling(fs)'s 32fs
		3.072	48kHz audio sampling(fs)'s 64fs
	O	1.536	48kHz audio sampling(fs)'s 32fs
		3.072	48kHz audio sampling(fs)'s 64fs
Slave	O	1.536	48kHz audio sampling(fs)'s 32fs
		3.072	48kHz audio sampling(fs)'s 64fs

The following figures indicates timing diagram of Audio CODEC Interface and SPI. Figure 15 shows timing diagram of audio interface. Each mode is defined in register map. Figure 16 shows timing diagram of SPI.

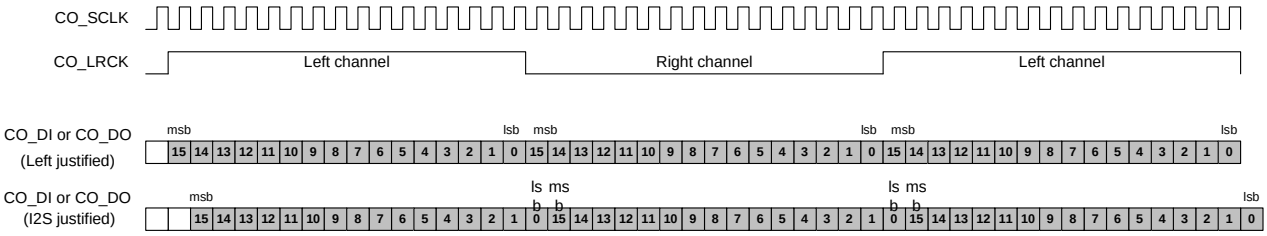
Figure 15. Audio Data Interface Timing Diagram



64fs mode,16bits format, CO_LRCK = 64 * CO_SCLK period



64fs mode,24bits format, CO_LRCK = 64 * CO_SCLK period



32fs mode,16bits format, CO_LRCK = 32 * CO_SCLK period

Figure 16. Master Mode SPI Timing Diagram

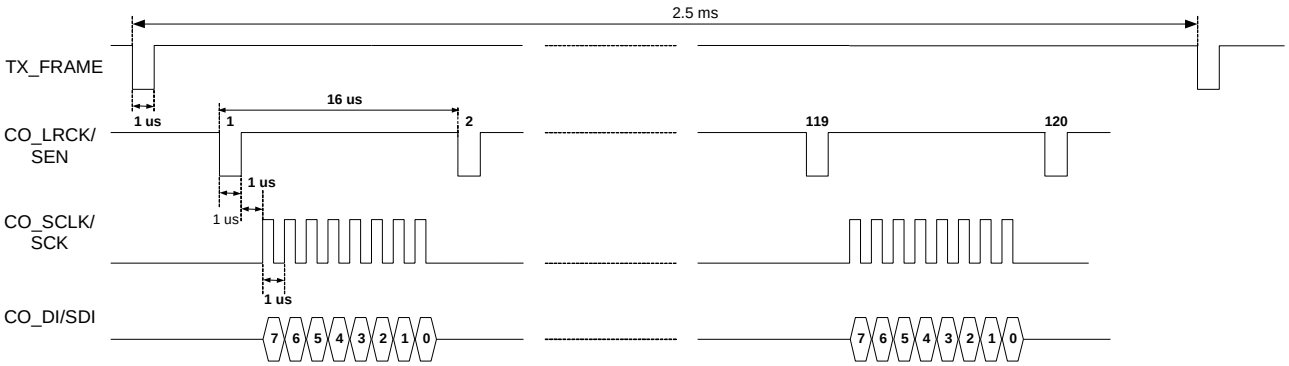


Figure 16 is timing diagram when DWM3000 outputs SCK and SEN signals in master mode. To transmit 120B data per frame, SEN and SCK signals are synchronous to TX_FRAME. According to SCK and SEN signals, DWM3000 receives 120B data per frame through SDI.

Figure 17. Slave Mode SPI Timing Diagram

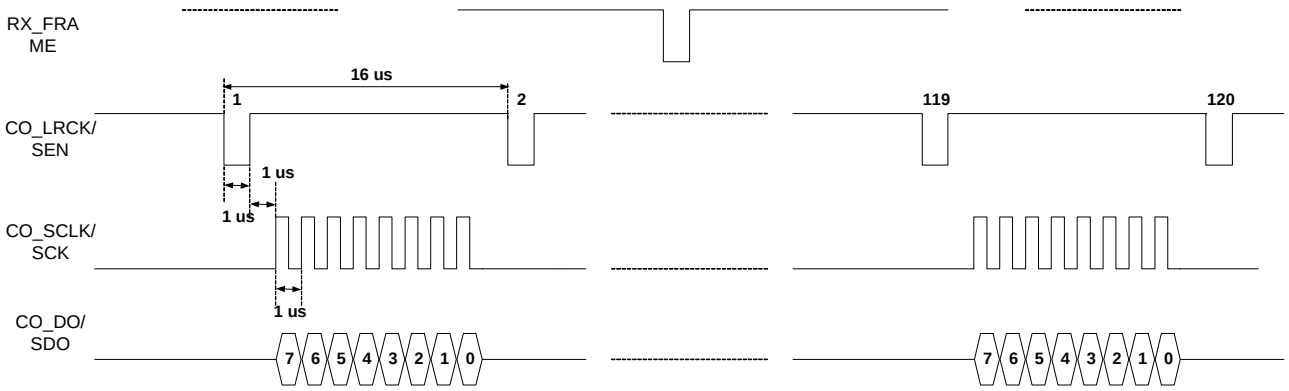


Figure 17 is timing diagram when DWM3000 outputs SCK and SEN signals in slave mode. To transmit 120 Bytes per frame, contrary to master mode, SEN and SCK signals are not synchronous to RX_FRAME. According to SEN and SCK signals, DWM3000 transmits 120B data per frame through SDO.

1.3.7 Baseband Pins

Table 11. Baseband Pin Description

PIN NAME	PIN Number	I/O	DESCRIPTION
MS_SEL	**18**	**DI**	This selects master/slave operation mode. [MS_SEL=1]: Master Mode [MS_SEL=0]: Slave Mode
REV_EN	**19**	**DI**	This selects P2P/Broadcasting operation mode. [REV_EN=1]: Point-to-Point Mode [REV_EN=0]: Broadcasting Mode
ID_SET	**17**	**DI**	This sets mode to transmit Device ID of chip from master system to slave system. To set transfer mode of Device ID, with DWM3000 reset, 'ID_SET' should be set to 1 in advance. When reset is released, Device ID transfer is performed. (In ID transfer progress, ID_SET should be kept for high.) After completing ID transfer successfully, DWM3000 transmits/receives data in predefined mode. If ID transfer is not desired, with DWM3000 being 'power off ' or reset, 'ID_SET' should be kept for low all the time. In general, before power on, set ID_SET to 1 and perform power on.
TX_FRAME	**15**	**DO**	This is a periodical signal indicating the beginning of transmit frame. Typically, 1us low pulse produces per 2.5ms. (The period 2.5ms allows a tolerance of 2us due to clock drift.)
RX_FRAME	**16**	**DO**	This is a periodical signal indicating the beginning of receive frame. Typically, 1us low pulse produces per 2.5ms. (In slave mode, the period 2.5ms allows a tolerance of 2us due to clock drift. In master mode, the period 2.5ms allows a tolerance of 3us due to clock drift.)
LOCK	**13**	**DO**	This signal indicates the status of DWM3000. It changes by a frame. In a receiver, it marks high in the frame interval where access code is detected.
ID_SET_FAIL	**14**	**DO**	In progress of transmitting Device ID from master system to slave system, in case Device ID transfer fails within predefined time, this signal is high. When a slave system saves the received Device ID into external EEPROM or MCU, transmitting Device ID is regarded success.
COMI_0, **COMI_1,** **COMO_0,** **COMO_1,** **COMIO_0,** **COMIO_1**	**42** **41** **40** **39** **38** **37**	**DI** **DI** **DO** **DO** **DIO** **DIO**	These signals are to transfer data via Pin-to-Pin. Within a frame of DWM3000, these are assigned to command field. The direction of COMIO_0 and COMIO_1 is controlled by defined parameters. Table 12 indicates pin mapping between these signals. It assumes that COMIO_0 and COMIO_1 are input signals at master mode. COMI, COMO and COMIO pins latch (input) or output signals every 2.5 ms intervals (DWM3000 frame unit). Therefore, input signals have to sustain their signals for at least 2.5 ms, and the pins maintain output signals for at least 2.5 ms. If there are any errors in the received frame, COMO[1:0] and COMIO[1:0] (if COMIO is set as output pin) pins all send output low during the respective frame.
FSEL_EN, **FSEL_0,** **FSEL_1**	**48** **45** **46**	**DI** **DI** **DI**	These signals select frequency of DWM3000. Table 2 shows the Frequency Selection Table using 'FSEL_EN' pins. In case of using external pins, only predefined fixed frequency is used. Cf. The other way to select a frequency is to save information of frequency into registers.

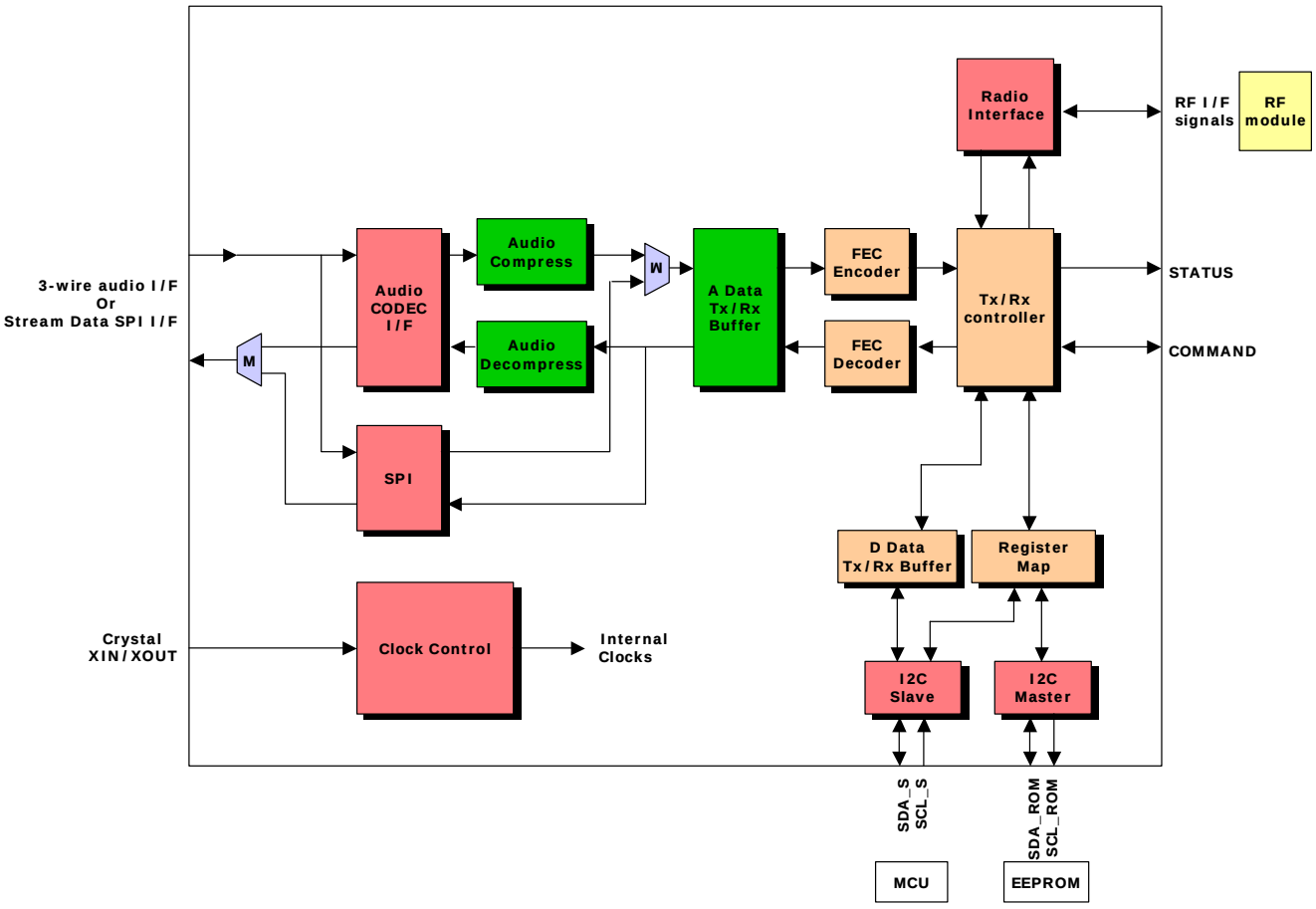
Table 12. COMI, COMO, COMIO Pin Mapping

Master		Pin to Pin Mapping	**Slave**	
Pin name	**I/O**		**Pin name**	**I/O**
COMI_0	Input	→	COMO_0	Output
COMI_1	Input	→	COMO_1	Output
COMIO_0	Input	→	COMIO_0	Output
COMIO_1	Input	→	COMIO_1	Output
COMO_0	Output	←	COMI_0	Input
COMO_1	Output	←	COMI_1	Input

2 FUNCTIONAL DESCRIPTION

This section provides explanation of DWM3000 in detail. It describes routines of transmit/receive, functional block, various operation mode, and so on.

Figure 18. DWM3000 Internal Block Diagram

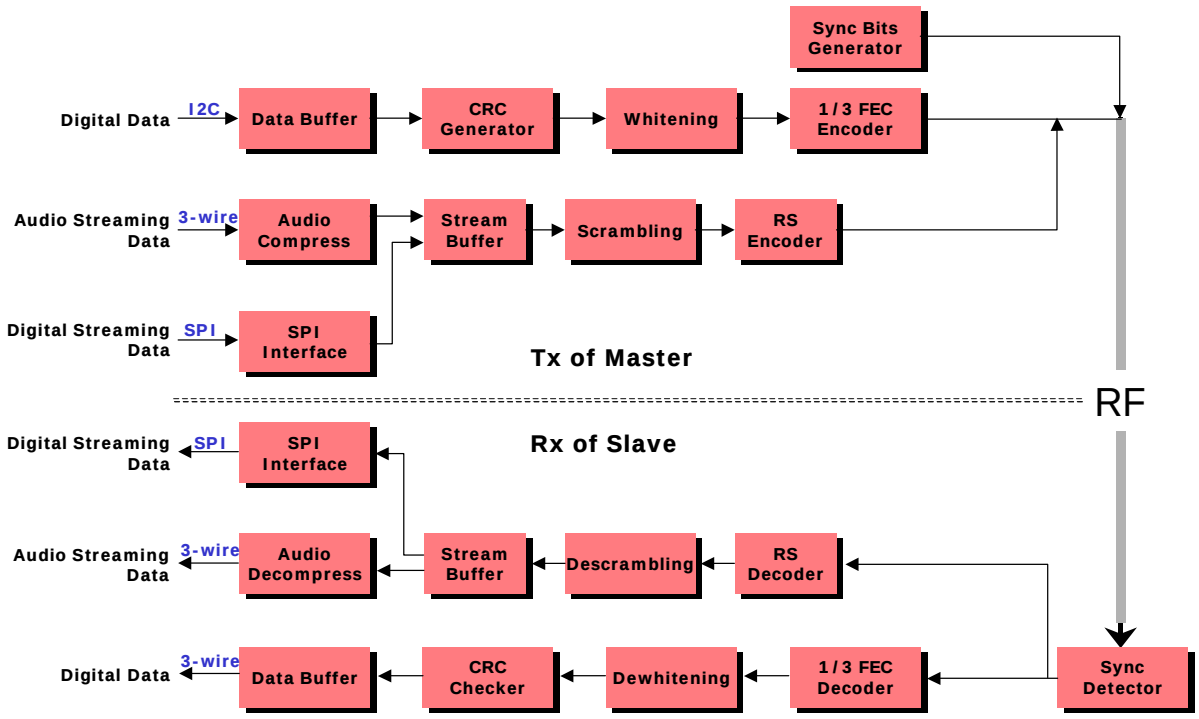


2.1 Transmit/Receive Routines

Transmit routines consist of digital data processing, audio streaming data processing, digital streaming data processing, data buffer, and stream buffer. To transmit digital data, DWM3000 communicates with MCU or EEPROM through I2C interface and transforms parallel data(bytes) to serial data(bits) after reading each byte stored in data buffer. Then this digital data will fly out after CRC generating, whitening, and 1/3 FEC. To transmit audio streaming data, DWM3000 communicates with external Audio CODEC through 3-wire audio interface and PCM audio data is compressed by audio compressor and stored in stream buffer. The compressed data will fly out after scrambling, and RS encoding. To transmit digital streaming data, DWM3000 communicates with external devices through SPI interface and stores the data in stream buffer. Then this digital streaming data will go through same FEC encoding routine of audio streaming data and fly out.

Receiver routines consist of digital data processing, audio streaming data processing, digital streaming data processing, data buffer, and stream buffer. To receive digital data, the received serial data is transformed parallel data after 1/3 FEC decoding, de-whitening, CRC checking and stored in data buffer. Then MCU will read this data through I2C interface. To receive audio streaming data, the received data is stored in stream buffer after RS decoding, and descrambling. Then external audio CODEC processes this decompressed data through 3-wire audio interface after decompressed by decompressor. To receive digital streaming data, the received data is stored in stream buffer through SPI interface after same FEC decoding routine of audio streaming data. Then external devices will read this streaming data through SPI interface.

Figure 19. DWM3000 Data Flow Chart



2.2 Audio CODEC Interface

DWM3000 supports 48/44.1㎑ audio data sampling rate. 44.1㎑ is available only for input of Master. Sampled data consists of 16 Bits PCM data for left and right channel. 48㎑ sampling is recommended for optimal performance. In 48㎑ sampling, DWM3000 may work as either a master or a slave for 3-wire Interface with external devices. Audio CODEC Interface supports direct interface and control between DWM3000 and external audio CODEC.

2.3 Radio Interface

DWM3000 Radio interface is purposed to connect directly to SiW1502 from Silicon Wave Inc. It will support Access Code detection, Gain Control and Initialization of SiW1502. Please refer to SiW1502 technical documents for more details.

2.4 FEC Encoder/Decoder

DWM3000 has two types of FEC(Forward Error Correction) block for digital data and Audio/Digital streaming data. For digital data, FEC block consists of CRC generator/checker, Whitening/De-whitening, and 1/3 FEC encoder/decoder. For Audio/Digital streaming data, FEC block consists of scrambler/descrambler and RS encoder/decoder for error-free data communication.

2.5 Clock Control

DWM3000 requires two master clocks. One is the Audio Master clock named as CO_MCLK, 12.288㎒ for audio communication. CO_MCLK pin is bi-directional. DWM3000 may use external system clock source through CO_MCLK. Otherwise, XIN/XOUT two input pins should be connected to external crystal oscillator. Then DWM3000 sends clock output through CO_MCLK. The other is BB_CLK, 16㎒ clock from external RF IC. Open Solution Co., Ltd. recommends SiW1502 from Silicon Wave Inc. as a reference RF IC. SiW1502 sends this 16㎒ clock to DWM3000 through BB_CLK.

2.6 Broadcasting Modes

DWM3000 supports broadcasting mode where multiple headphones or speakers can hear same music simultaneously together. In broadcasting mode, single master and multiple slaves exist in the same link whereas single master and single slave exist in Point-to-Point mode. Only one slave can communicate bi-directionally with the master in Broadcasting mode.

Figure 20. Broadcasting Modes

2.7 Master/Slave Mode

DWM3000 may operate as either a master or a slave. Master sends audio stream data or digital stream data through RF IC. The other hand, Slave receives audio stream data or digital stream data and sends control data to Master. Master uniquely exists in each link. Multiple slaves can exist in broadcasting mode. The level of MS_SEL can select each device as Master or Slave. In MS_SEL=0, DWM3000 becomes Slave. Otherwise MS_SEL=1, DWM3000 becomes Master.

2.8 Variable Modes of Frequency Operation

DWM3000 supports three types of Spread Spectrum using external Bluetooth RF IC. This was adopted to avoid any interference with other devices that use 2.4GHz frequency range or from the environment. The three types of Spread Spectrum supported are Frequency Hopping Spread Spectrum (FHSS), Adaptive Frequency Selection (AFS), and Fixed Channel mode.

FHSS refers to the conventional 79 channels (or 23 channels, dependent on the country of use) hopping of Bluetooth by SiW1502 that works perfectly in pair with DWM3000. But device using this hopping method receives a lot of interference from other devices that use 2.4GHz range frequency such as WLAN, and also from other Bluetooth devices that resides near it. FHSS, being built to avoid interfering with other devices, rather interferes a lot with devices that has high output power using 2.4GHz frequency range and with other FHSS devices. Therefore, DWM3000 also has adopted improved frequency hopping method called AFS developed by OS.

During the initialization, DWM3000 scans 79 channels (or 23) and selects the clear, non-interfered, and reliable channel and starts the communication between the master and slave. During the channel link, if the channel becomes unreliable and the error detection from FEC block exceeds the preset error threshold value, DWM3000 executes setup scanning, as in initialization, and reselects new clear and reliable channel. This is AFS. Through this method, high quality wireless audio can be achieved by avoiding any interference from WLAN, and other 2.4GHz frequency range devices.

FHSS and AFS can be selected by setting appropriate parameters in the EEPROM. For those who desire to use only certain range of frequencies, DWM3000 can operate at the frequency range when channel range parameters are written to the appropriate area in the EEPROM with FSEL_EN=0.

In the Fixed Channel mode, 4 frequency levels can be selected by setting FSEL_EN to 1 and setting FSEL_1 and FSEL_0 to 00 for 2.410GHz, 01 for 2.430GHz, 10 for 2.450GHz, and 11 for 2.470GHz.

2.9 Device ID Set

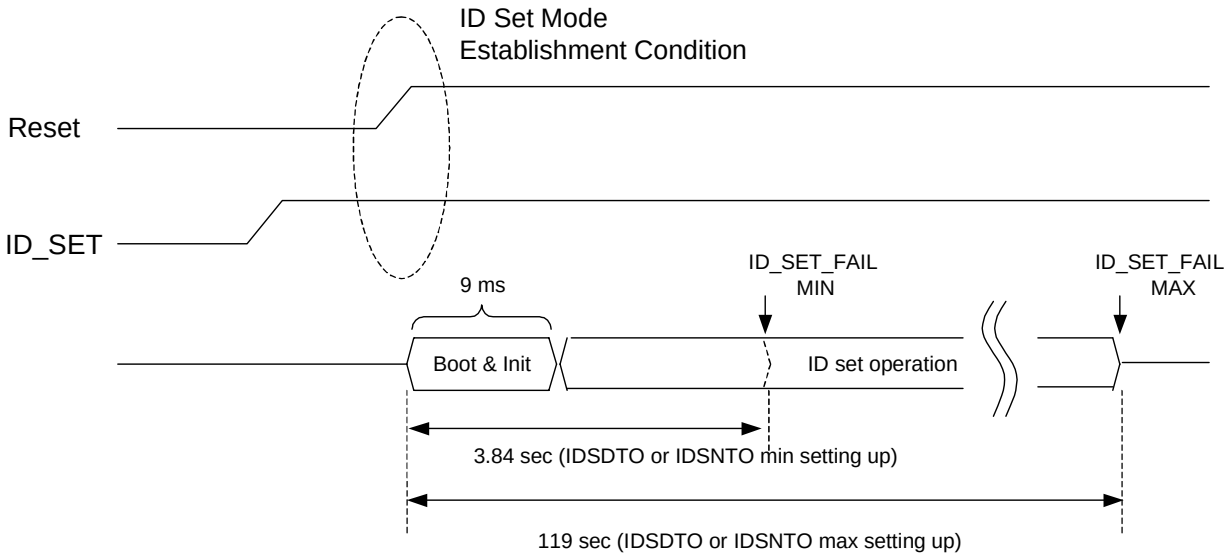
To establish communication channel properly, hopping frequency and Syncword of each packet should be determined by Device ID(Identification). Device ID is unique value of each device, master and slaves. Only master and slaves with same Device ID can communicate each other. Device ID can be set manually in case selected master and slaves do not communicate together. This procedure is “Device ID set”. Device ID set procedure occurs when master and slave devices boot simultaneously with ID_SET=1. In this procedure, the slave can figure out the Device ID of the master and store it in external EEPROM.

When ID_SET is established, DWM3000 performs ID send/scan to send Device ID of master to slave before general page operation. In normal mode, communication is accomplished by going into page state directly without ID send/scan.

Figure 21 shows timing between Reset and ID_SET in ID_SET mode. Additionally, it shows timing outputting ID_SET_FAIL signal when ID_SET operation fails.

Parameter register’s Timeout values during ID_SET procedure decide the time when ID_SET_FAIL signal appears. The values are dependent on master or slave mode. In master mode, the value is IDSDTO(0x11) in parameter register. In slave mode, the value is IDSNTO(0x12) in parameter register. Figure 21 illustrates mininum/maximum time when ID_SET_FAIL signal is shown according to IDSDTO and IDSNTO.

Figure 21. ID_Set_Mode and ID_Set_Fail Timing Diagram



2.10 Power Saving Scan

When the communication link is lost, the slave starts scanning procedure to re-establish the lost link. If the slave cannot find the master within a certain amount of time stored in and read from external EEPROM, the slave automatically goes to power saving mode.

3 RESET & INITIALIZATION

Figure 22. DWM Initialization Sequence

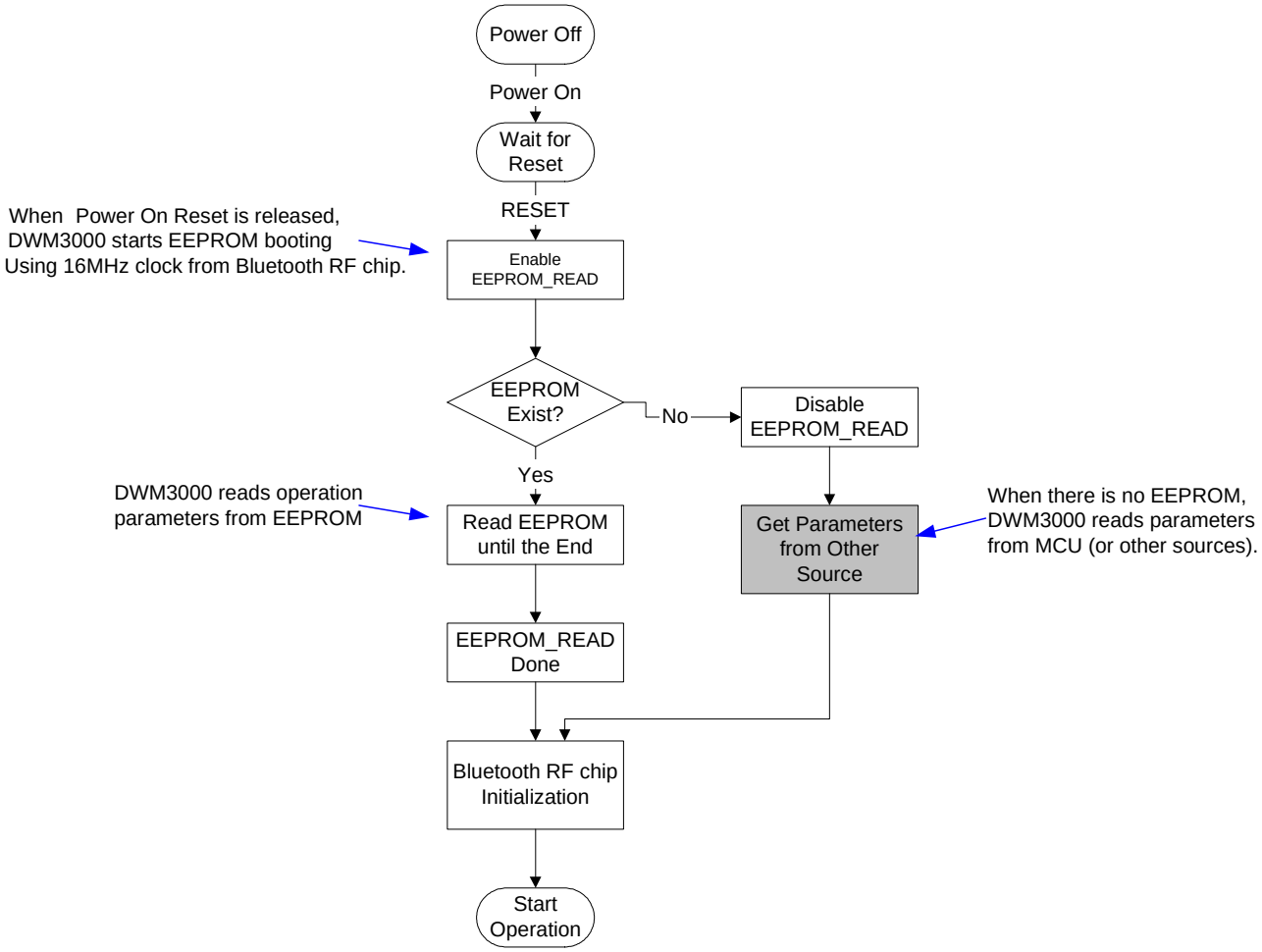


Figure 23. Normal EEPROM Booting Timing Diagram

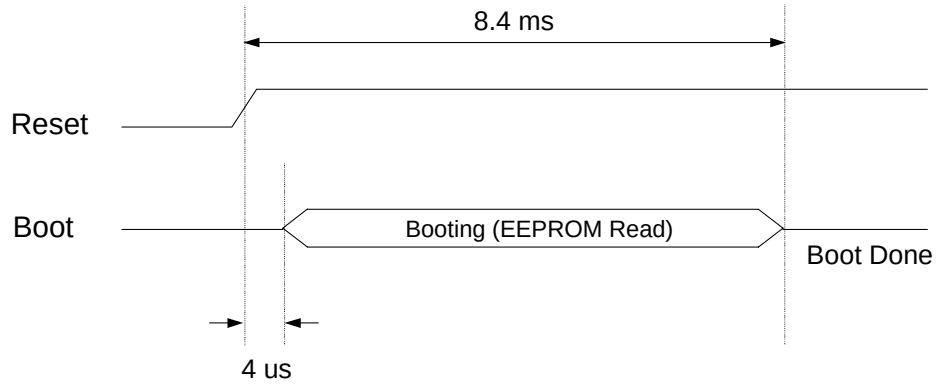


Figure 23 shows the time when DWM3000 loads normally boot parameters from external EEPROM during booting operation.

Figure 24. EEPROM Detect Fail Timing Diagram

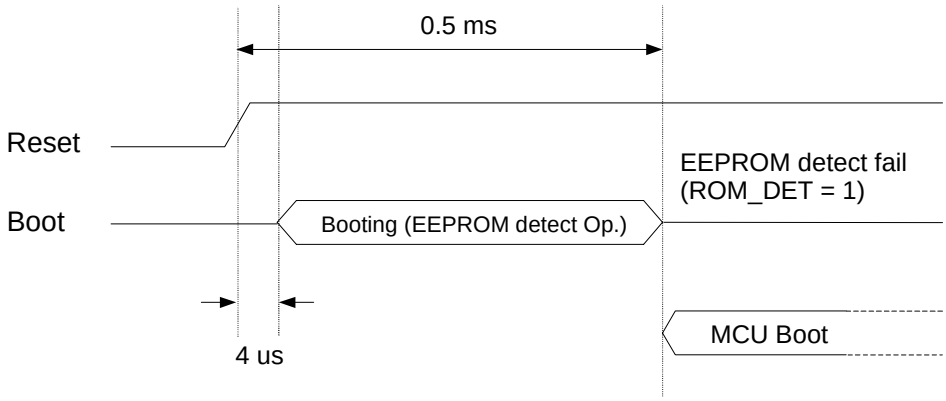


Figure 24 shows boot fail timing in case there is no EEPROM or EEPROM's recognition pattern does not coincide with predefined pattern.

4 SPECIFICATIONS

This section describes allowable maximum voltage, current, and temperature. Additionally, it provides DC/AC electrical characteristics.

Table 13. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage4	3.6	V
V_{IN}	DC Input Voltage	4.6	V
I_{latch}	Latch-up current	±200	μA
T_{STG}	Storage Temperature	-65 to 150	°C

Table 14. DC Electrical Characteristics

Symbol	Parameter	MIN	TYP	MAX	Unit
V_{DD}	Supply Voltage	2.3	2.5	2.7	V
V_{SS}	Supply Voltage		0		V
V_{DDIO}	IO Supply Voltage	3.0	3.3	3.6	V
V_{SSIO}	IO Supply Voltage		0		V
V_{IH}	High Level Input Voltage	2.0			V
V_{IL}	Low Level Input Voltage			0.8	V
V_{OH}	High Level Output Voltage	2.4			V
V_{OL}	Low Level Output Voltage			0.4	V
I_{IH}	High Level Input Current	-10		+10	μA
I_{IL}	Low Level Input Current	-10		+10	μA
I_{OP}	Supply Current in Normal state		20		mA
T_A	Commercial Temperature Range	0		70	°C

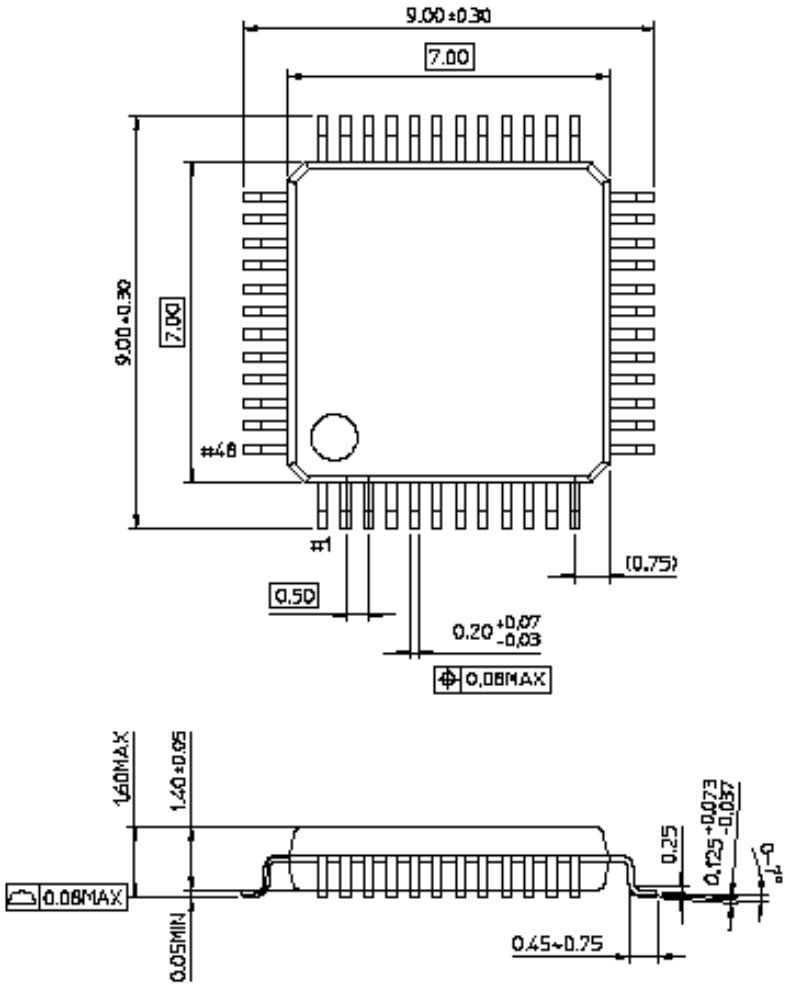
Table 15. AC Electrical Characteristics

Symbol	Parameter	MIN	TYP	MAX	Unit
XIN	Input clock frequency		12.288		MHz
F_{offset}	Input clock offset		TBD		ppm
T_{reset}	Minimum reset pulse width	183			ns

5 PACKAGE DIMENSION

This section indicates packet dimension of 48-PIN LQFP (Dimensions in Millimeters)

Figure 25. 48-PIN LQFP



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