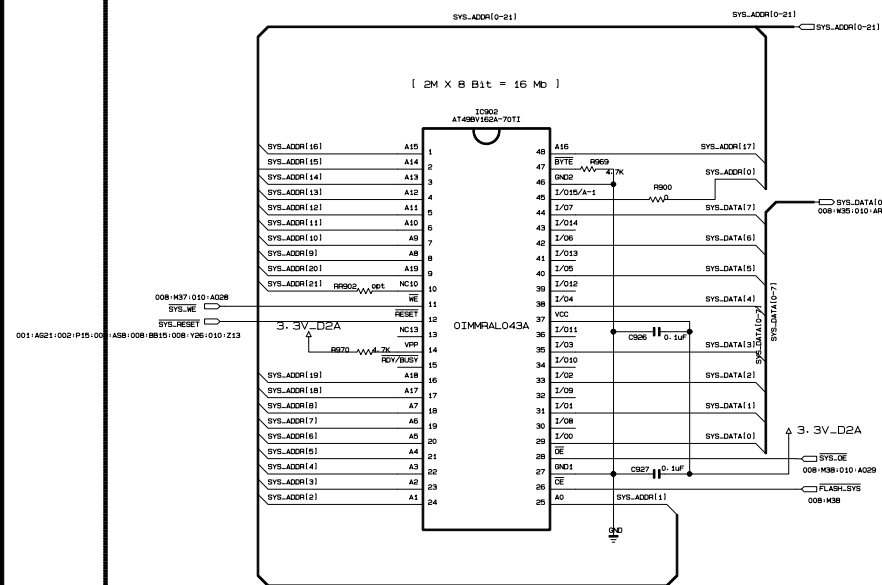
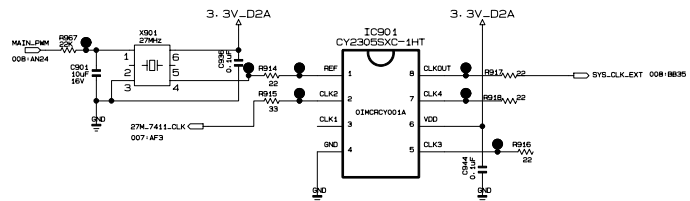


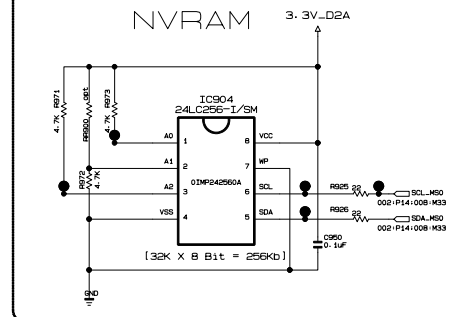
Flash ROM 2MBytes



PLL Clock



NVRAM



DDR MEMORY

comments
 ==> Register and capacitor values used in the this sheet will be fixed after impedance match test
 ==> Some Termination and serial registers was deleted after pre-simulation test of DDR interface. 06/02/201

