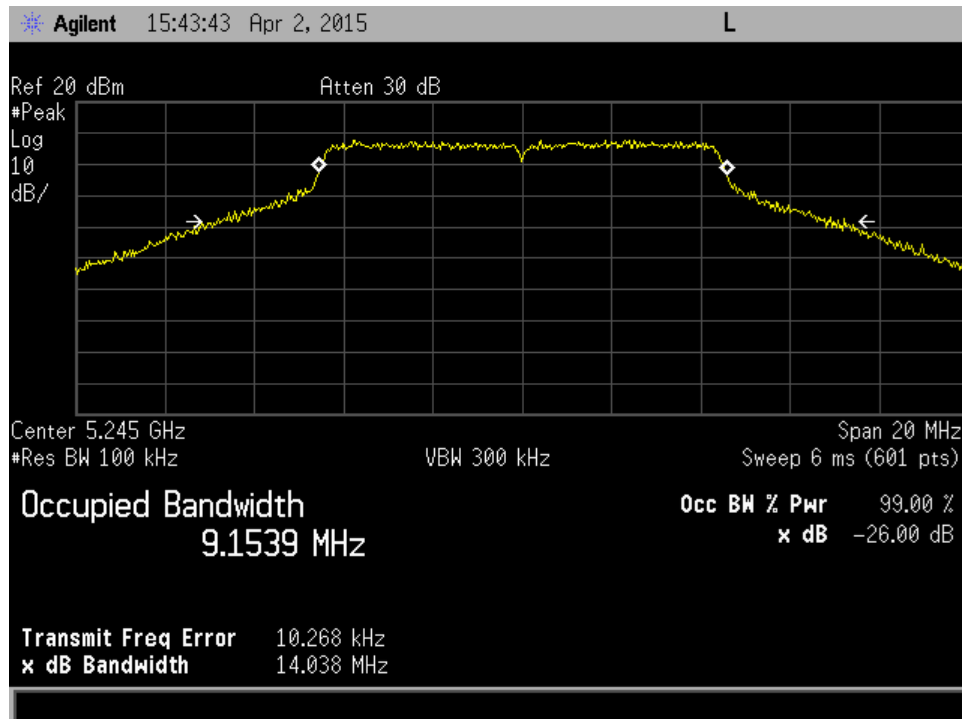


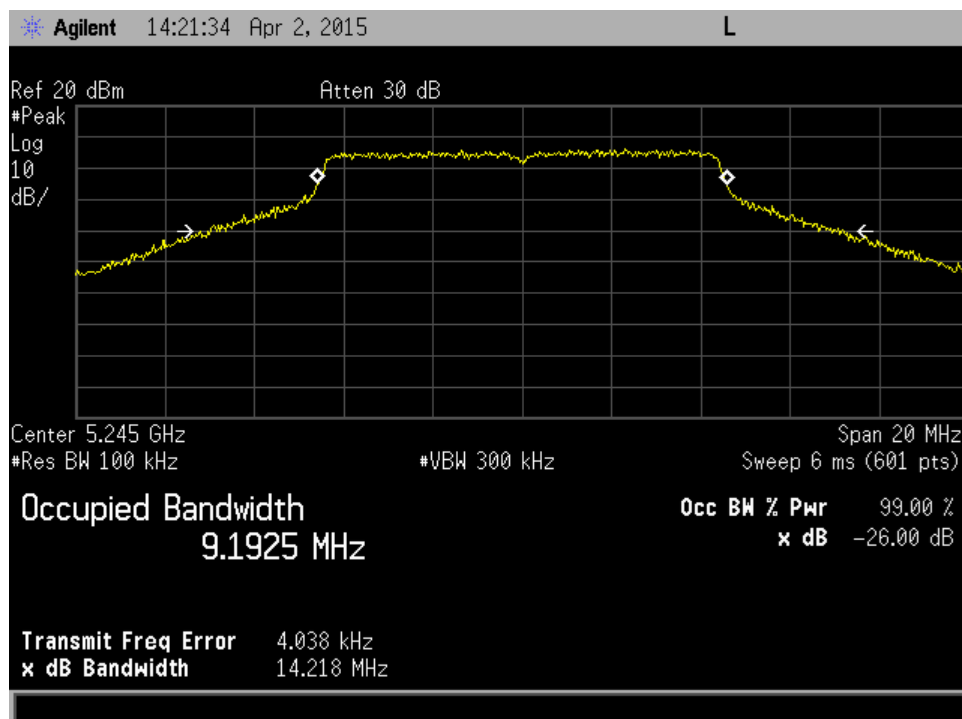
# **Annex D**

## **Occupied Bandwidth**

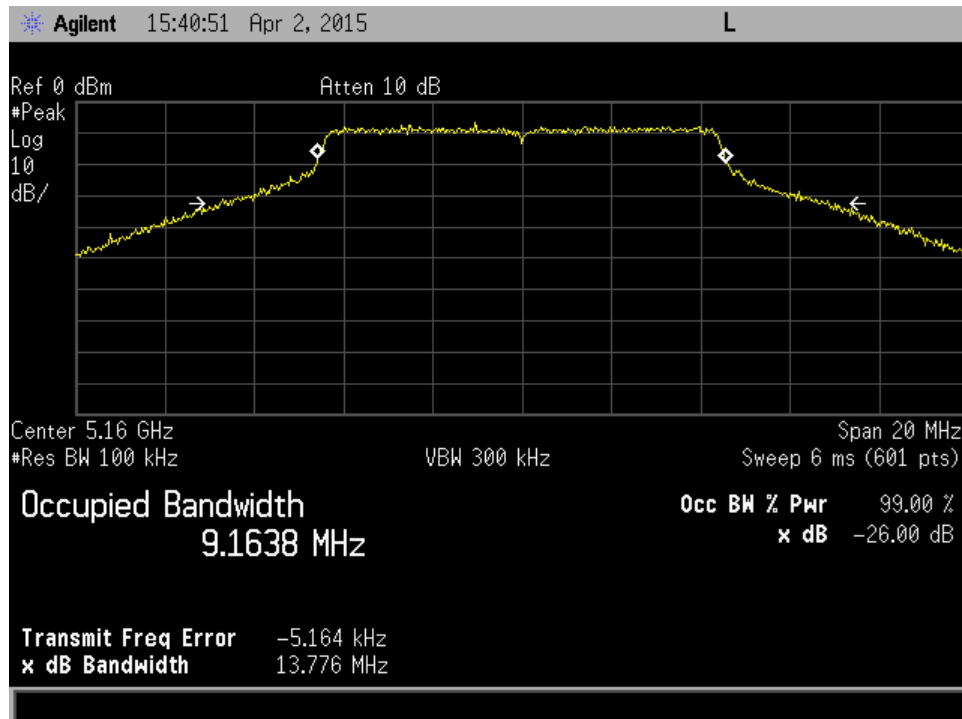
### **Ports J7 and J8**



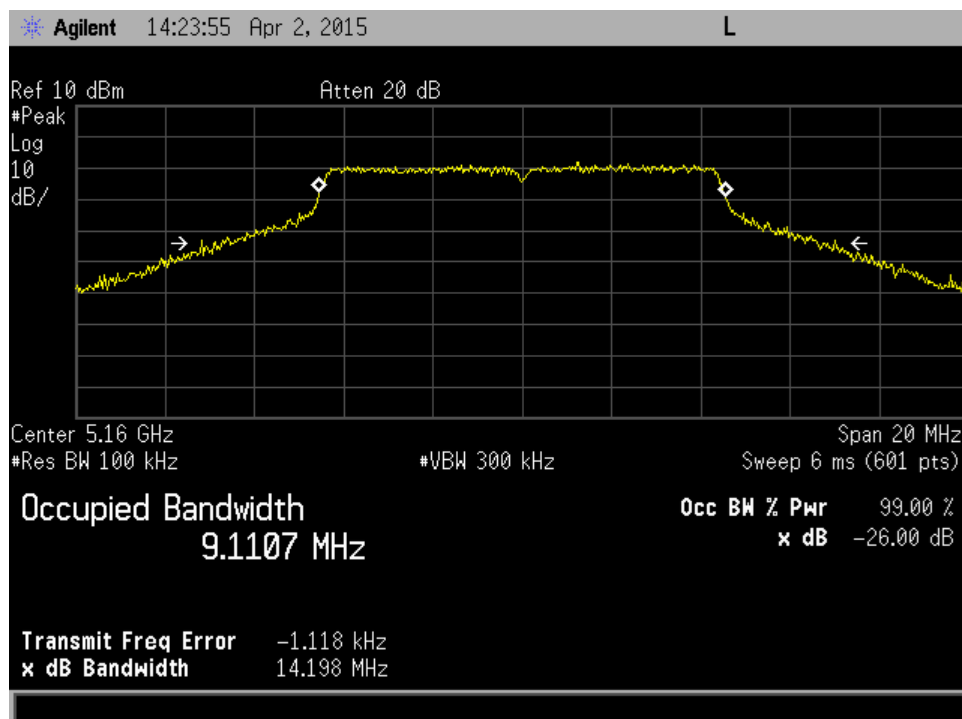
10MHz high ch J7



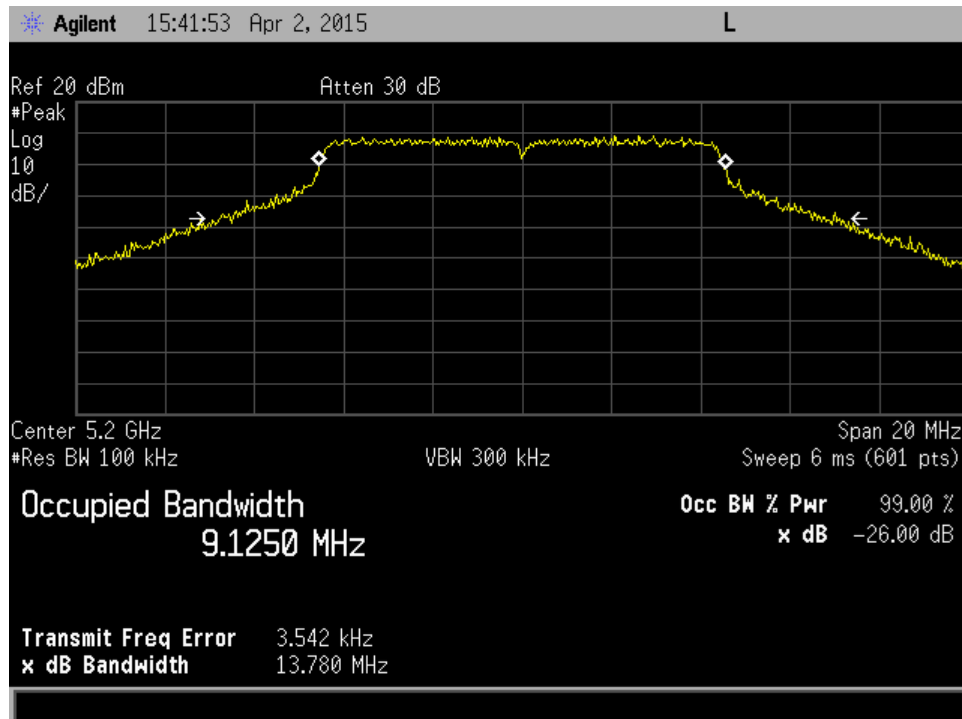
10MHz high ch J8



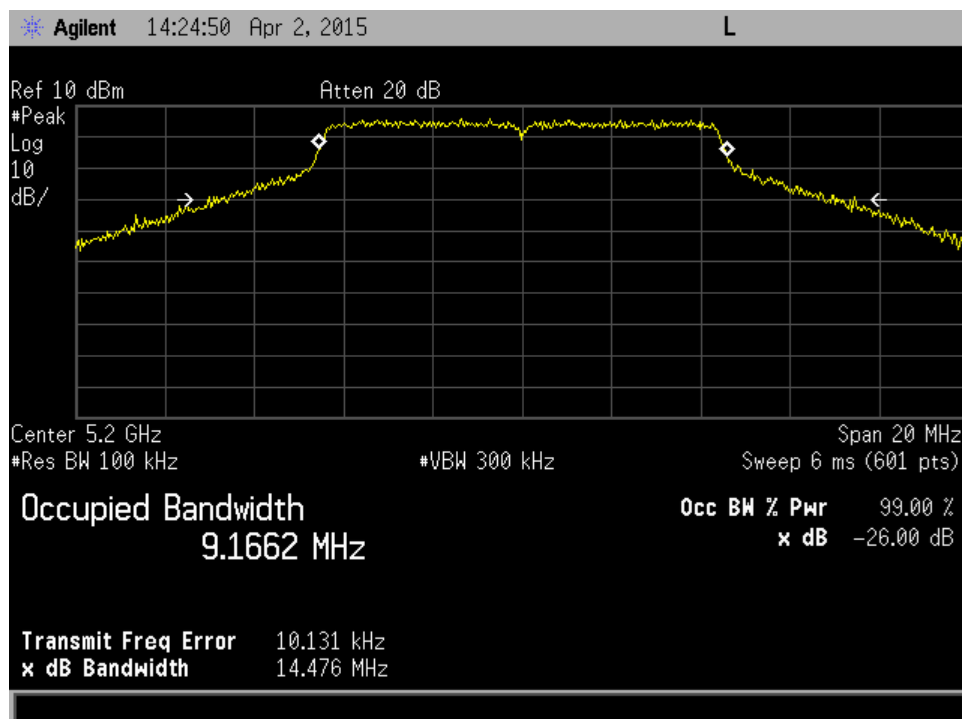
10MHz low ch J7



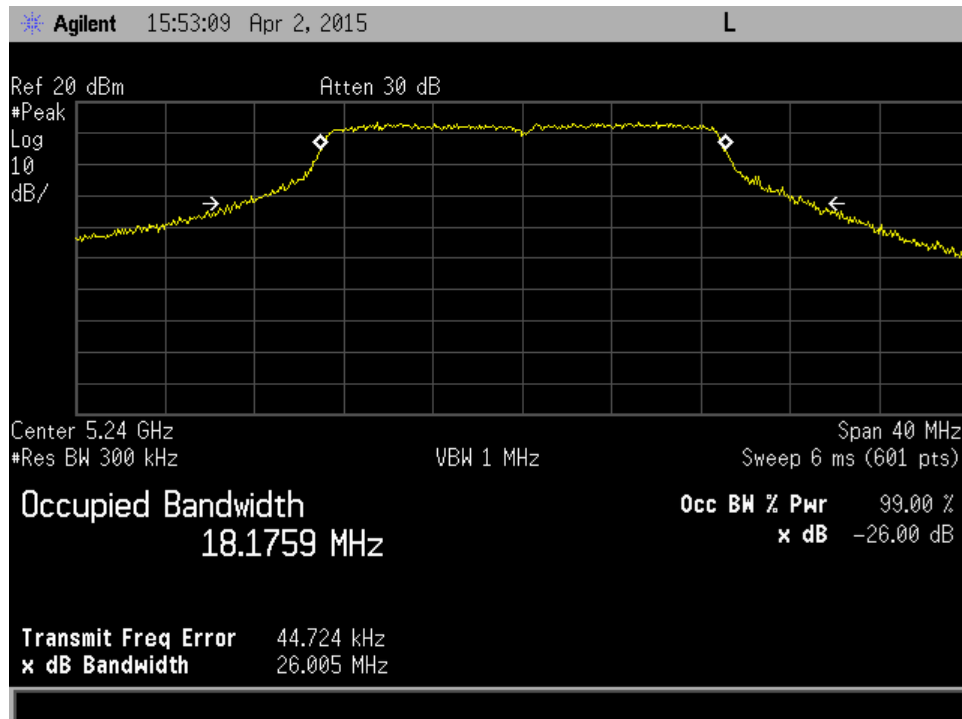
10MHz low ch J8



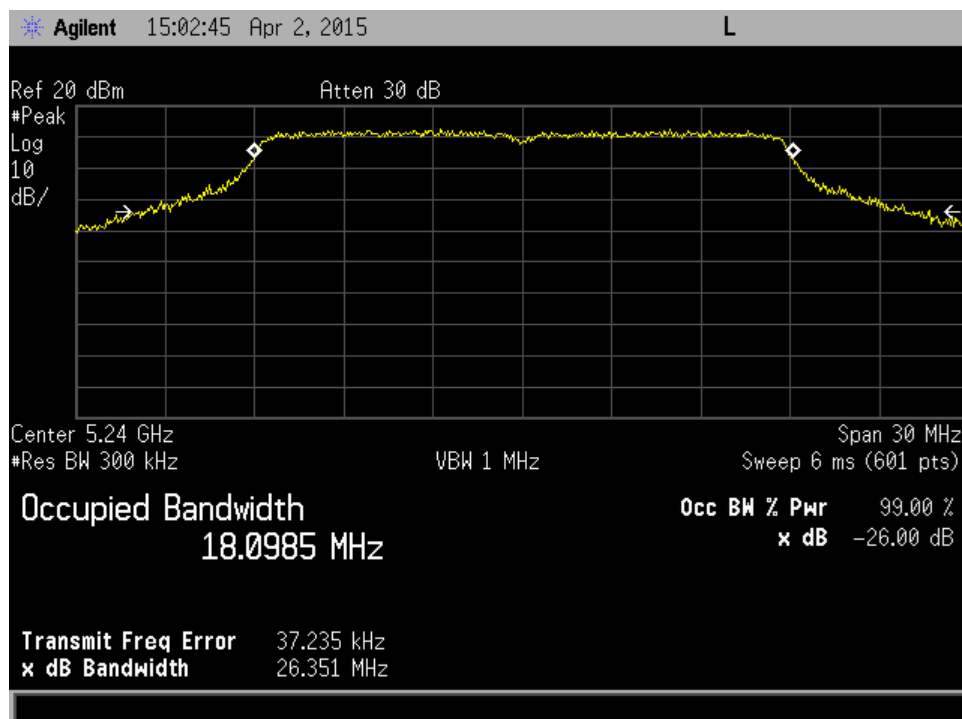
10MHz mid ch J7



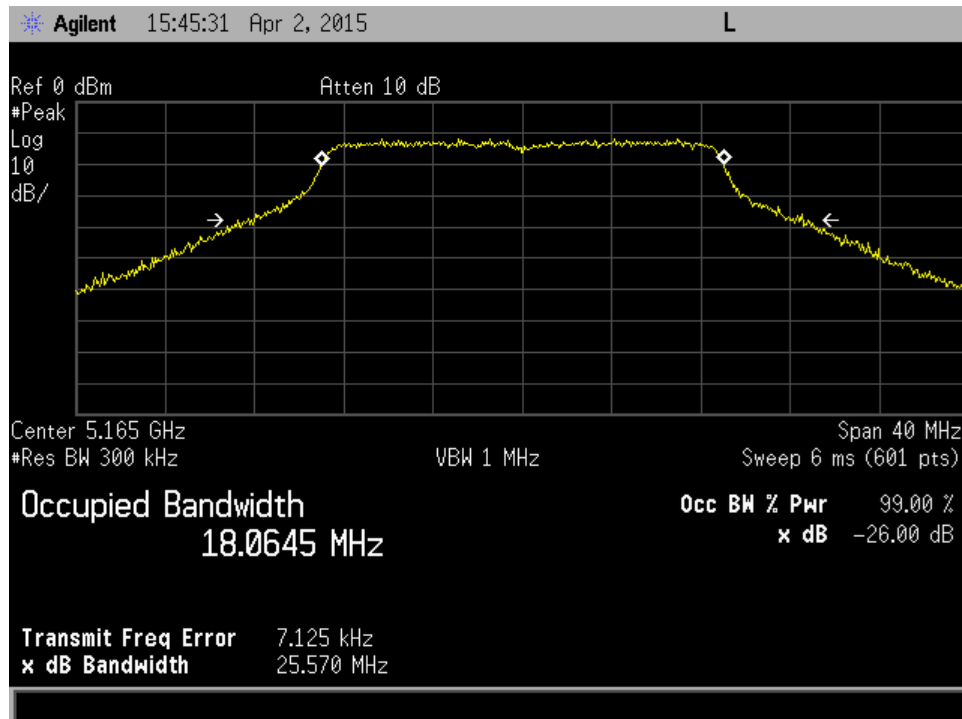
10MHz mid ch J8



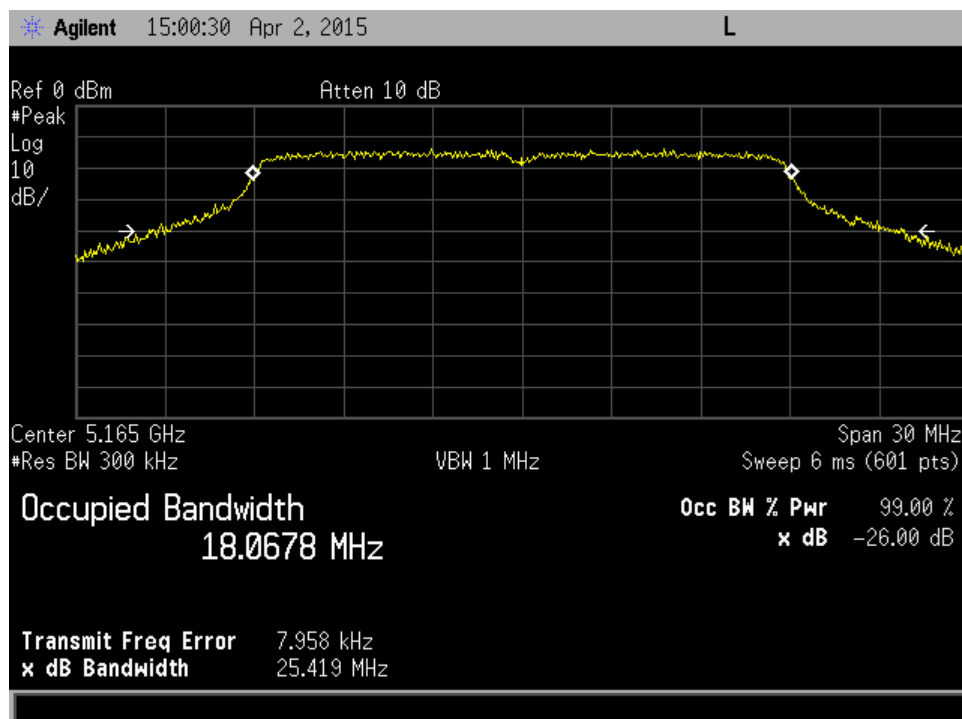
20MHz high ch J7



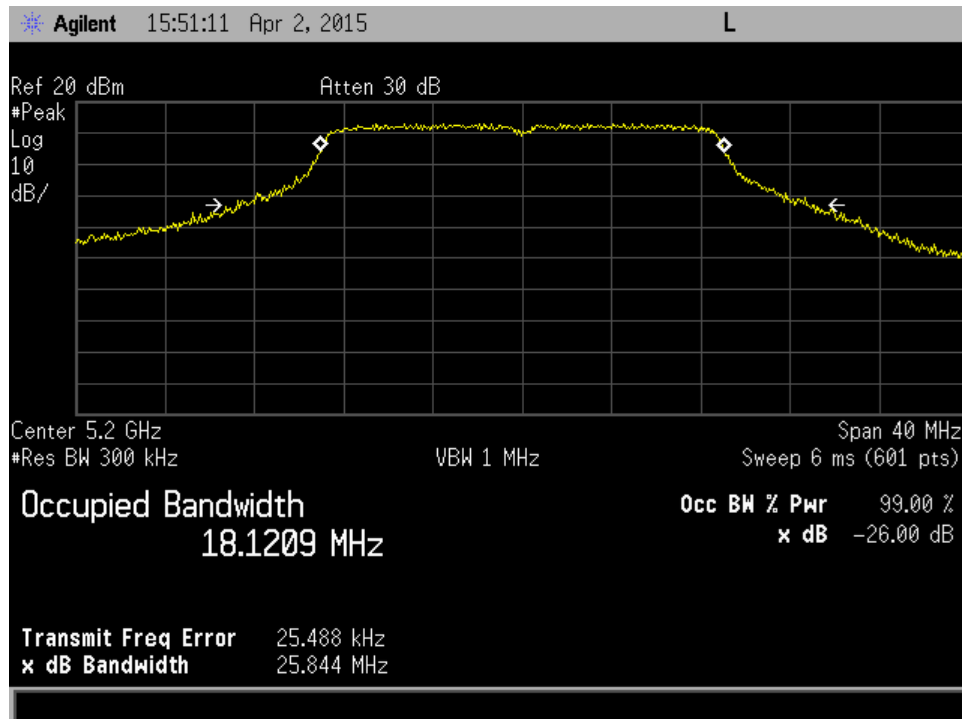
20MHz high ch J8



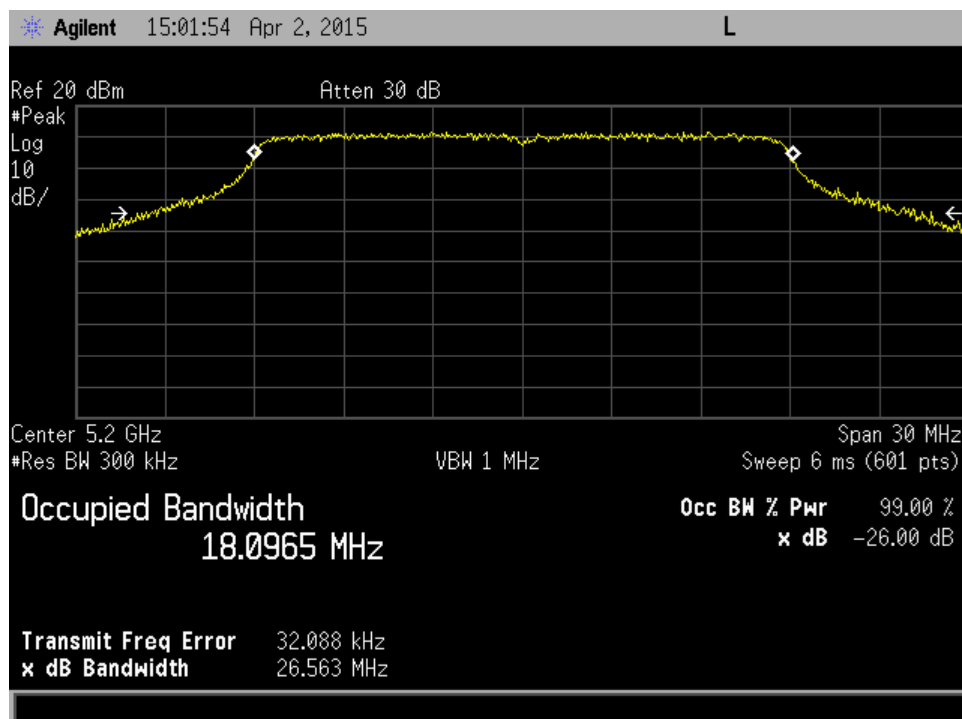
20MHz low ch J7



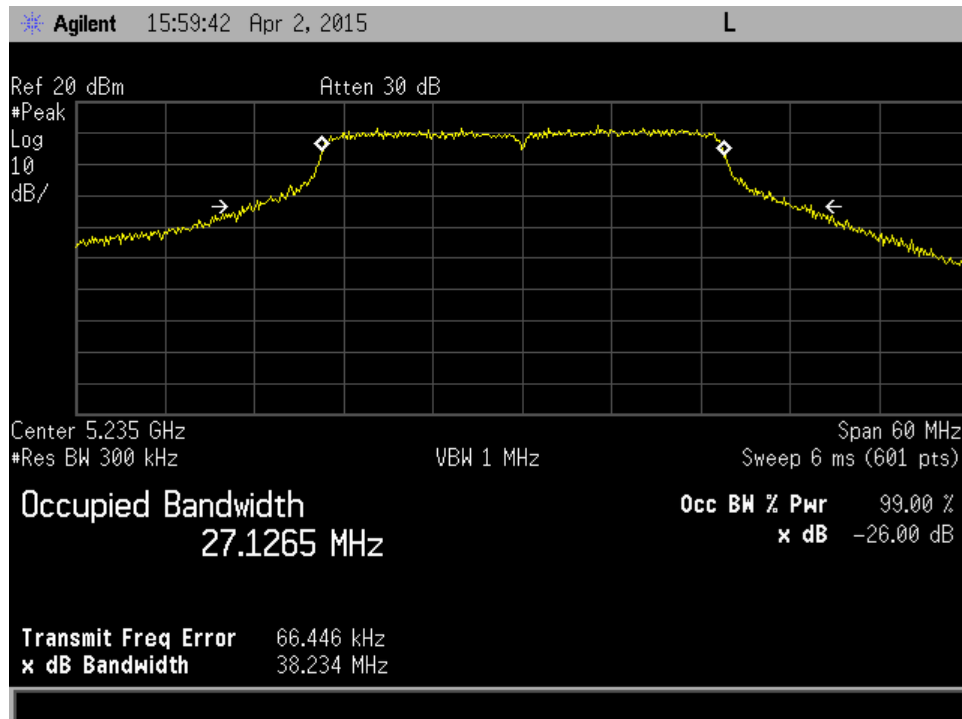
20MHz low ch J8



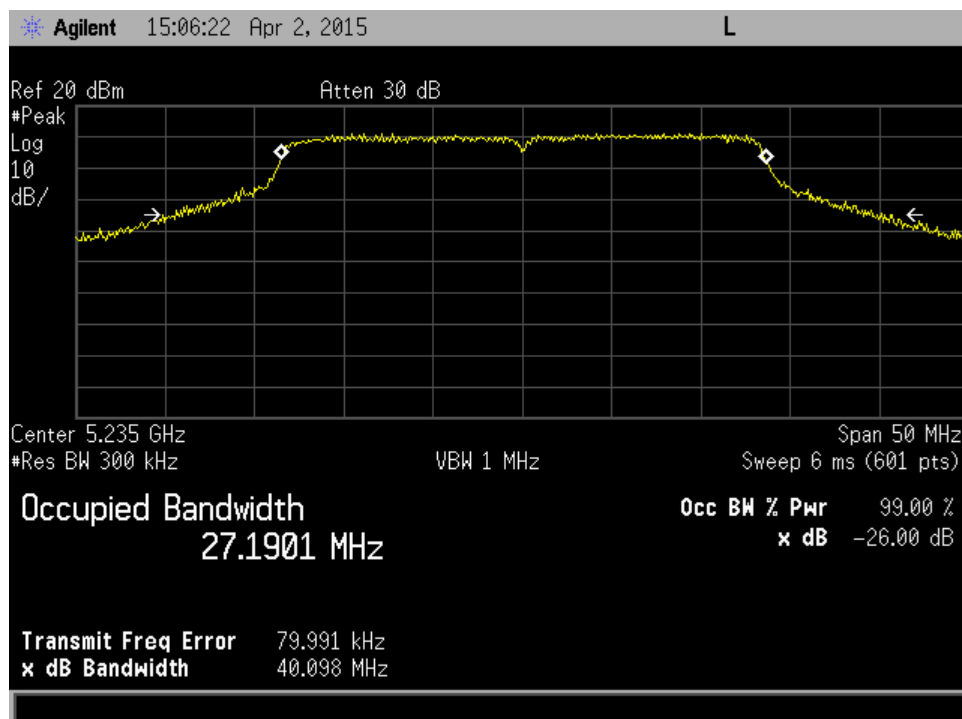
20MHz mid ch J7



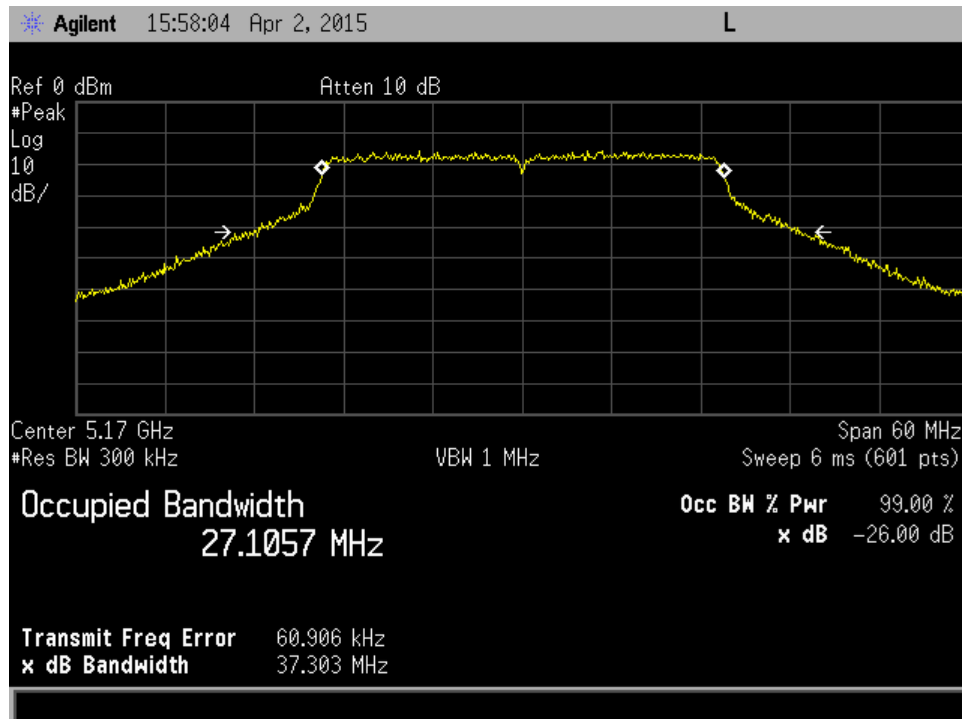
20MHz mid ch J8



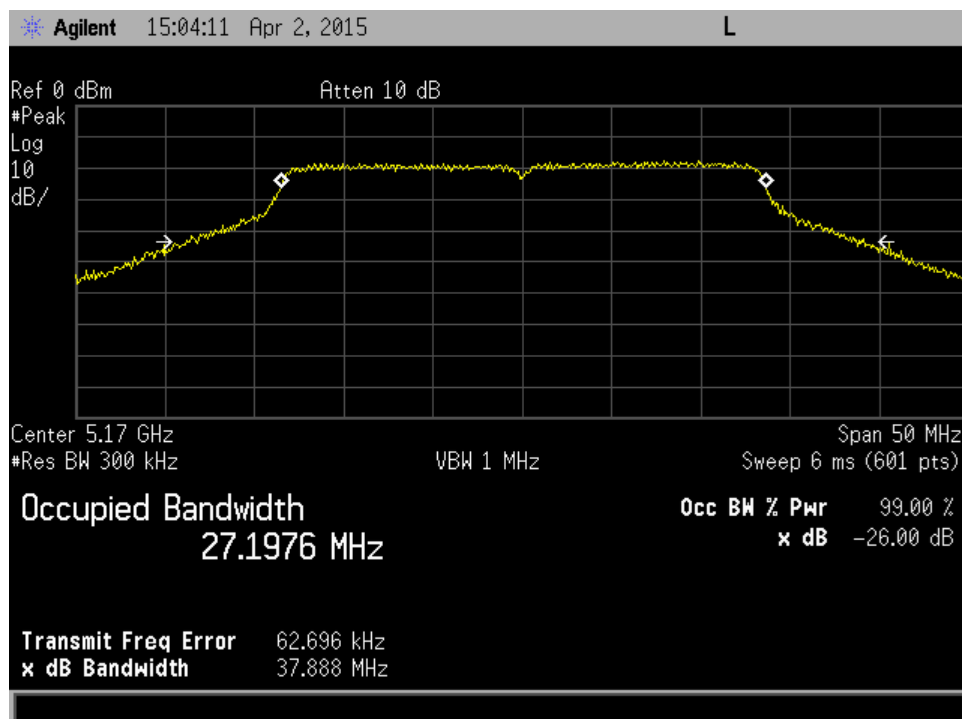
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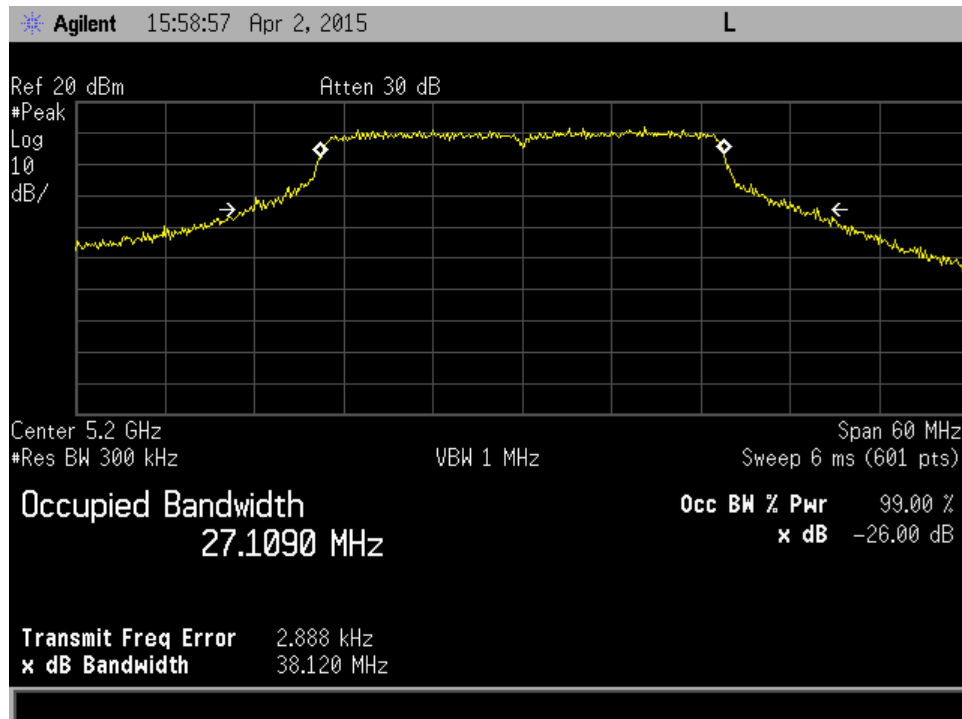
30MHz high ch J8



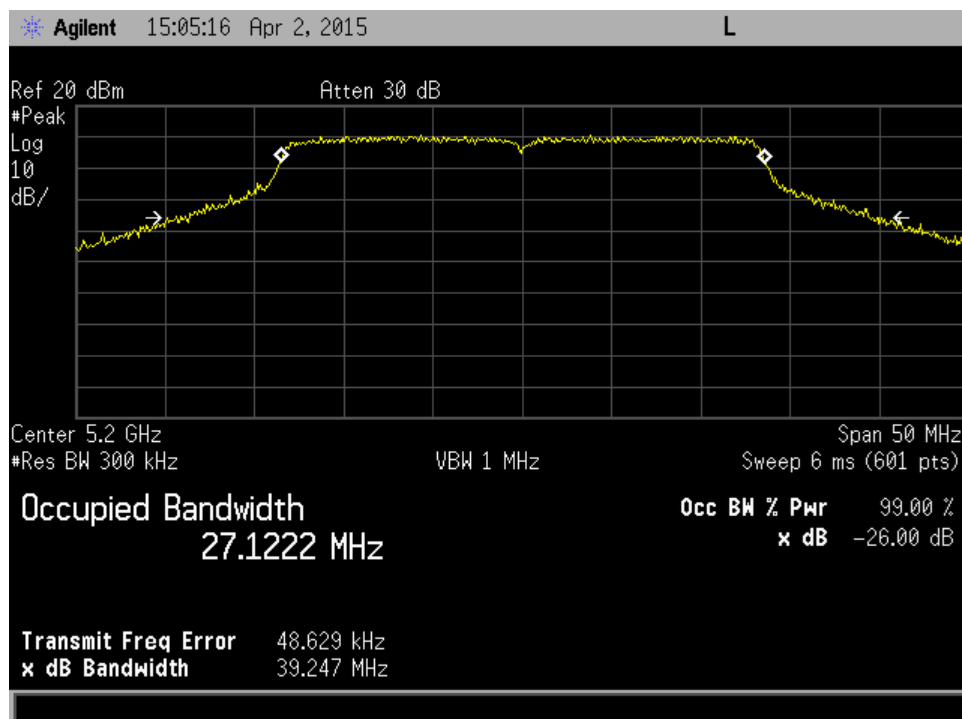
30MHz low ch J7



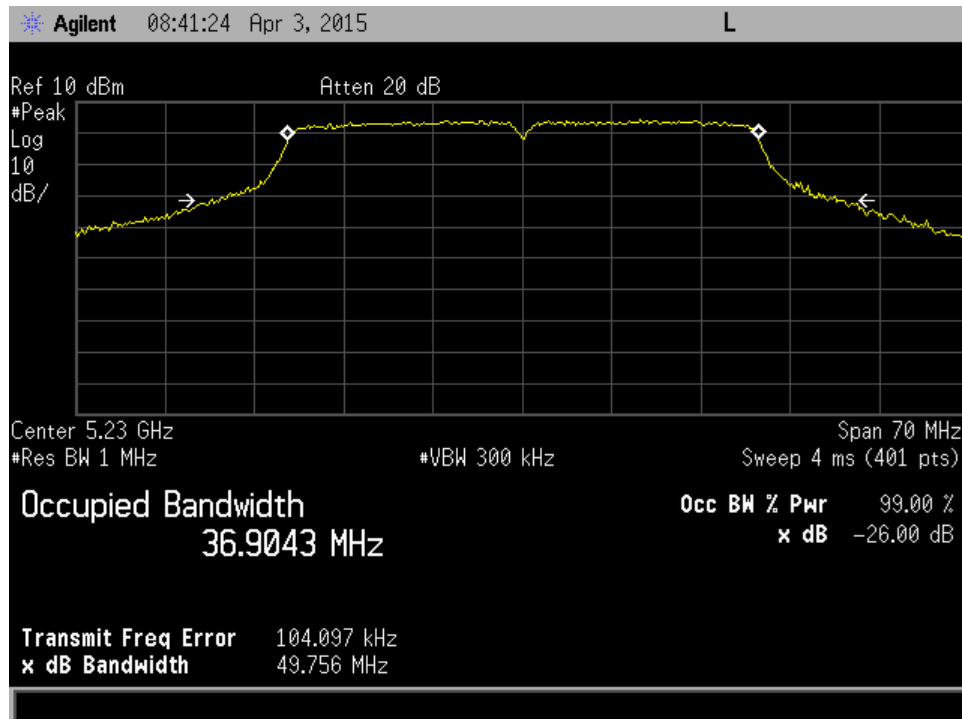
30MHz low ch J8



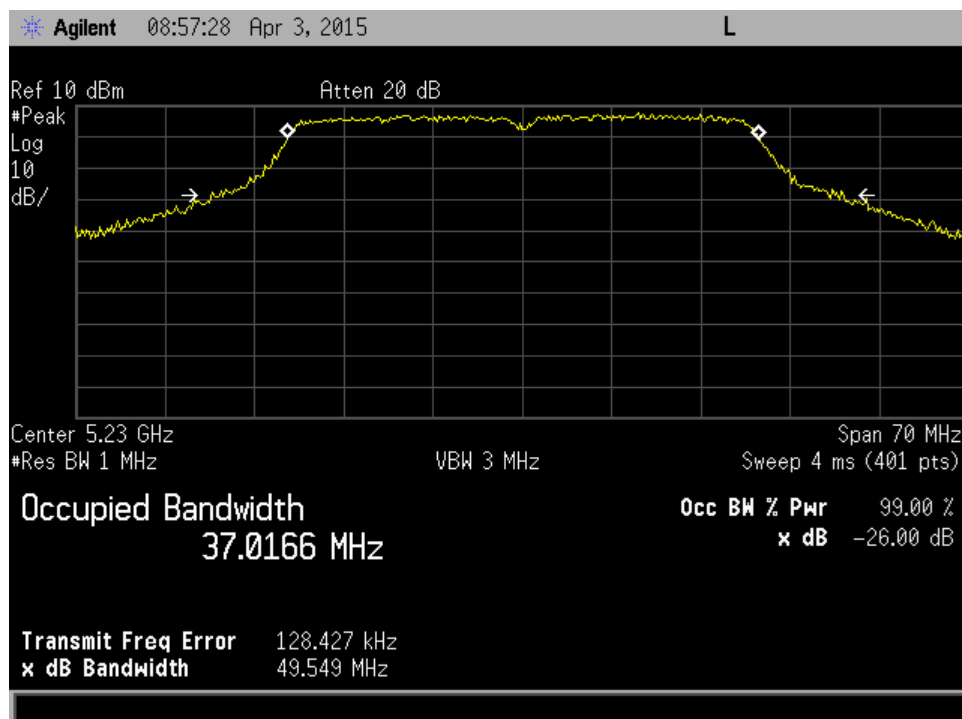
30MHz mid ch J7



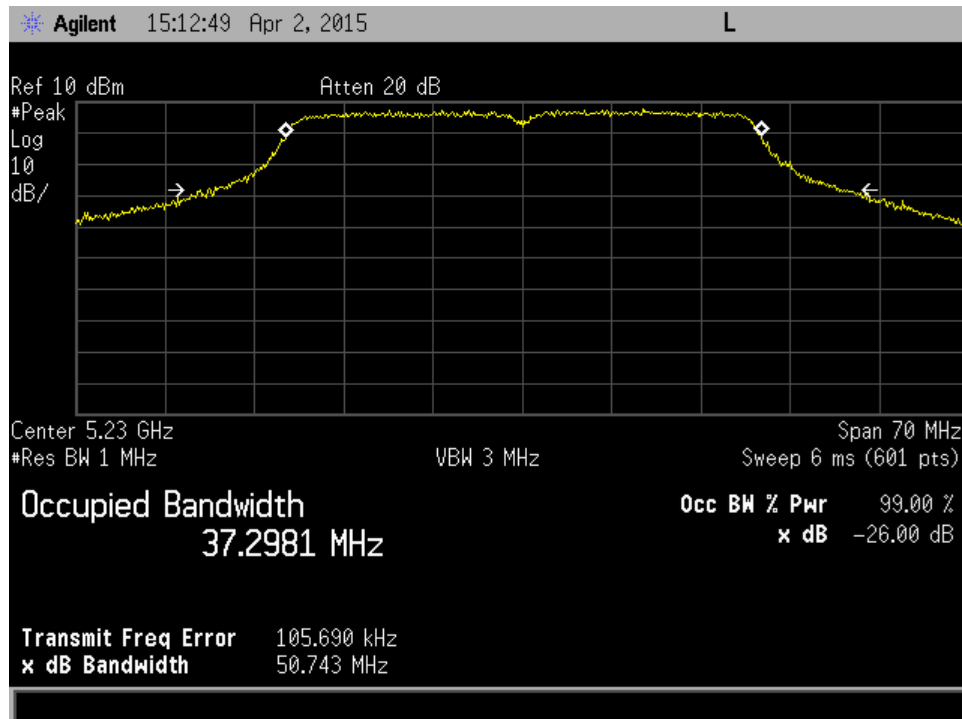
30MHz mid ch J8



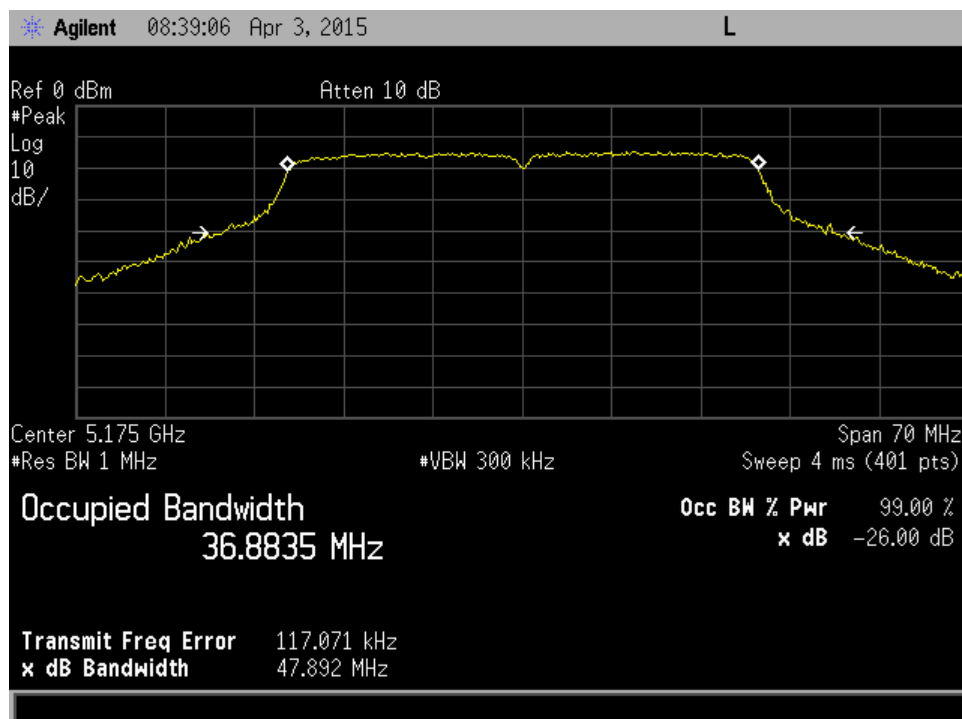
40MHz high ch J7



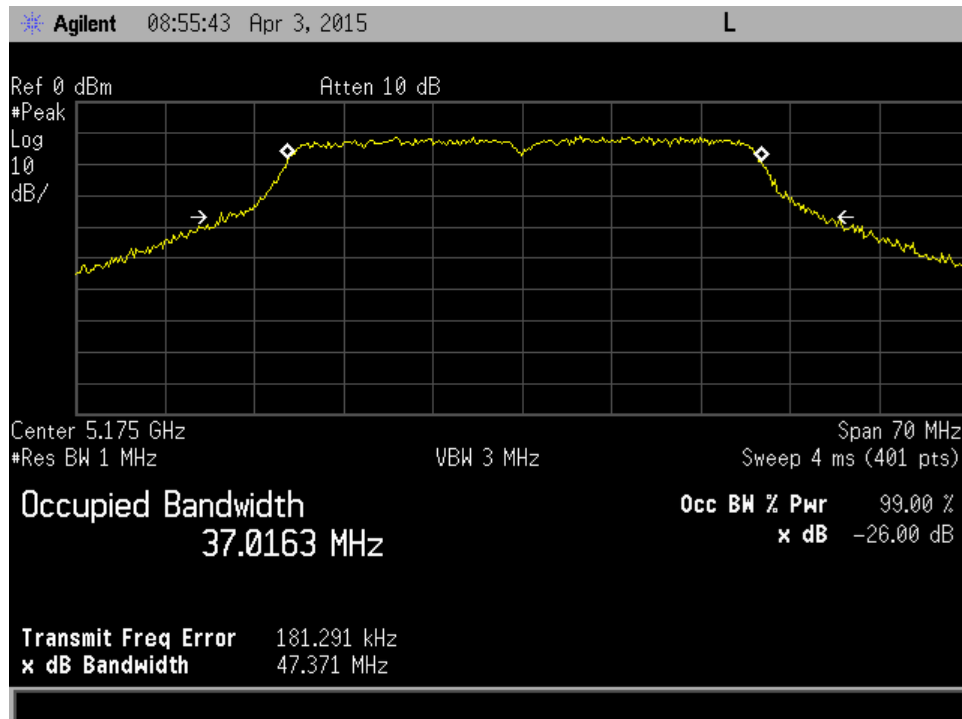
40MHz high ch J7\_



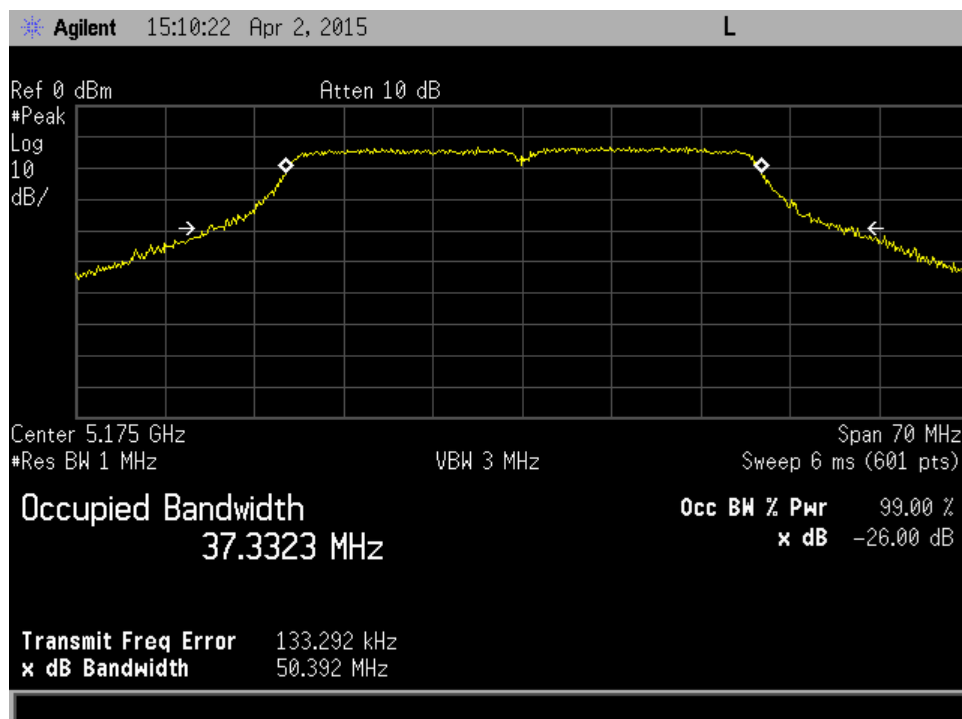
40MHz high ch J8



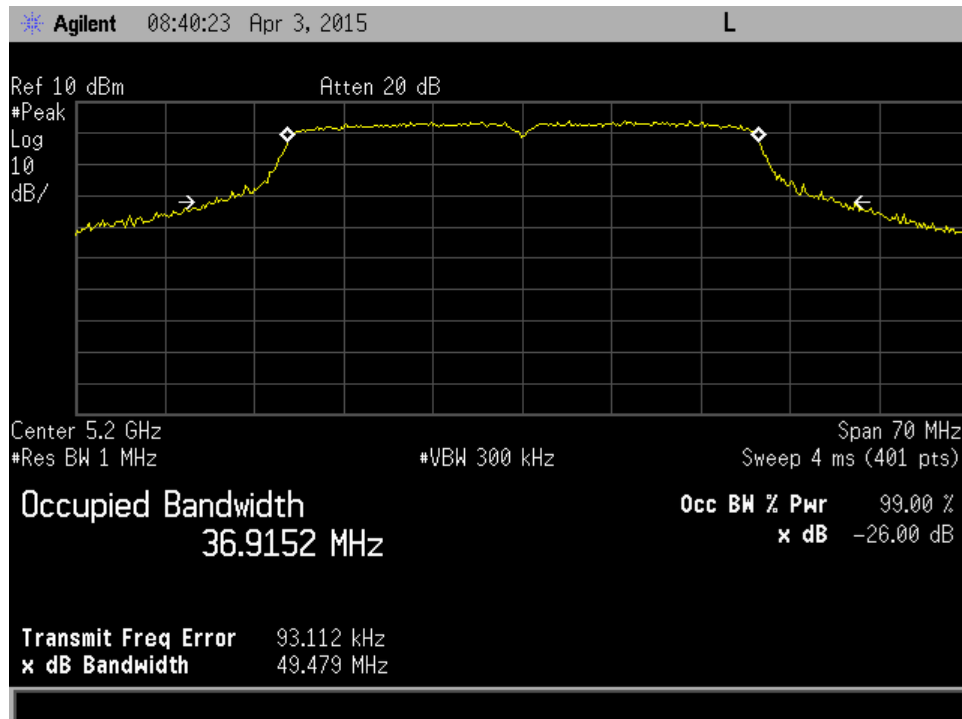
40MHz low ch J7



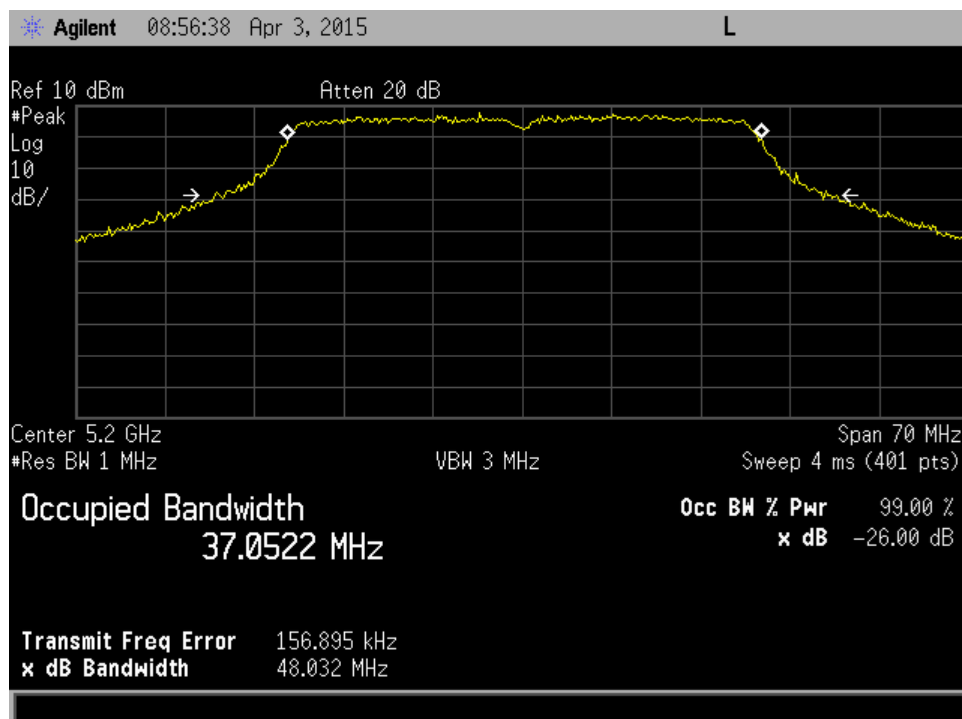
40MHz low ch J7\_



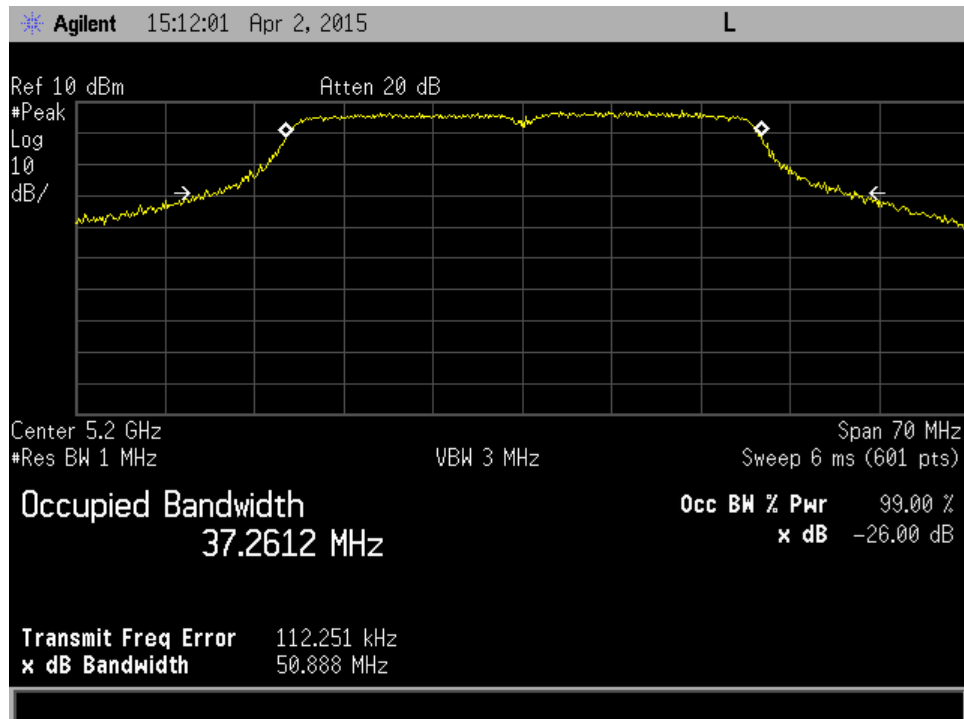
40MHz low ch J8



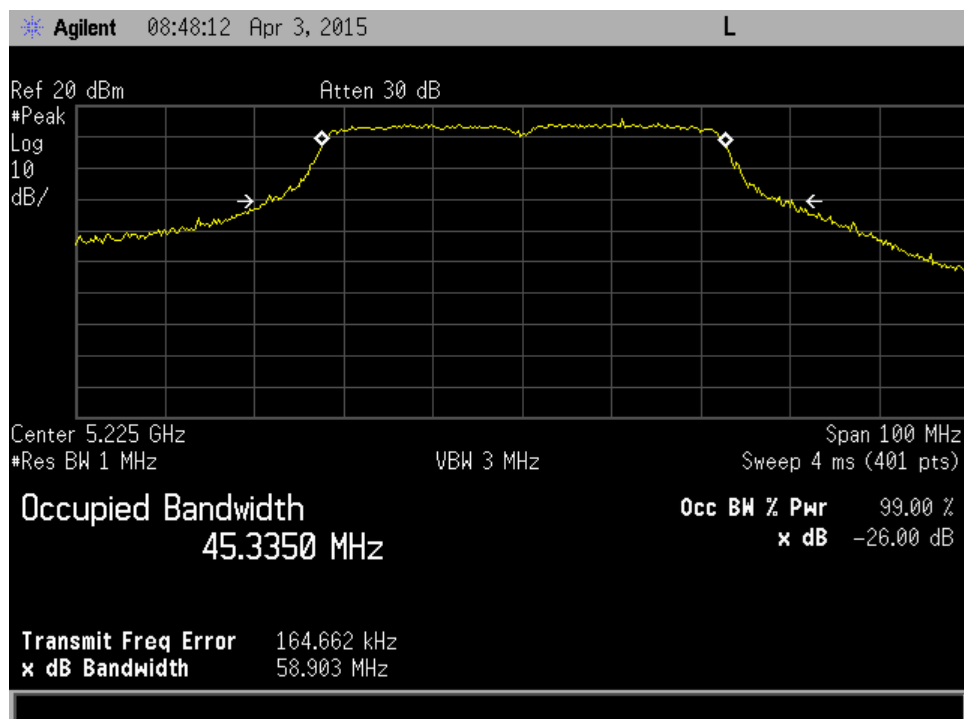
40MHz mid ch J7



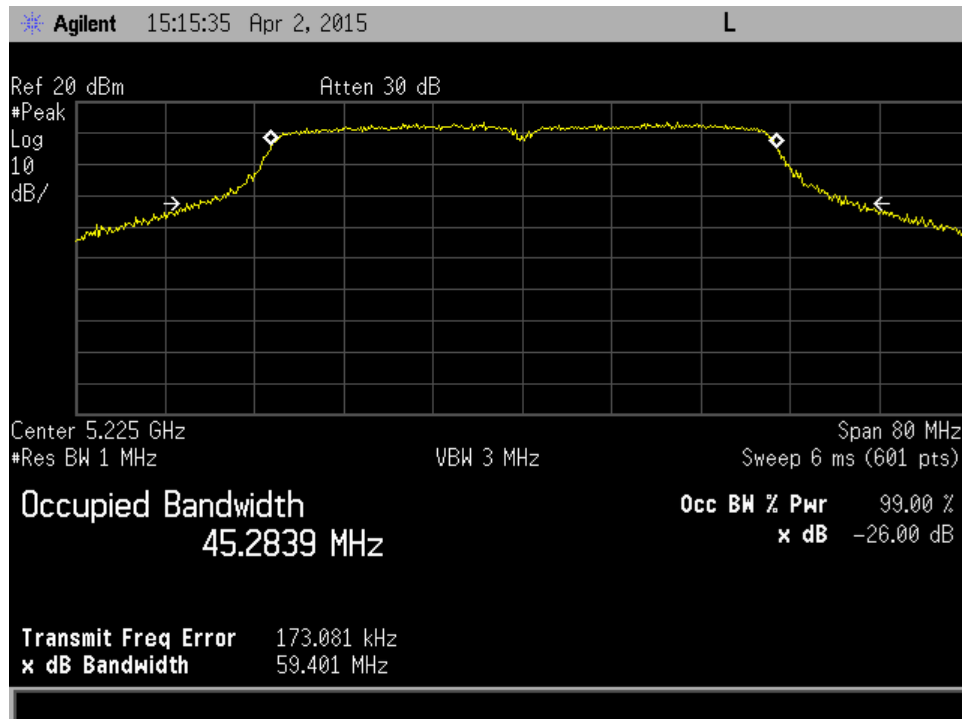
40MHz mid ch J7\_



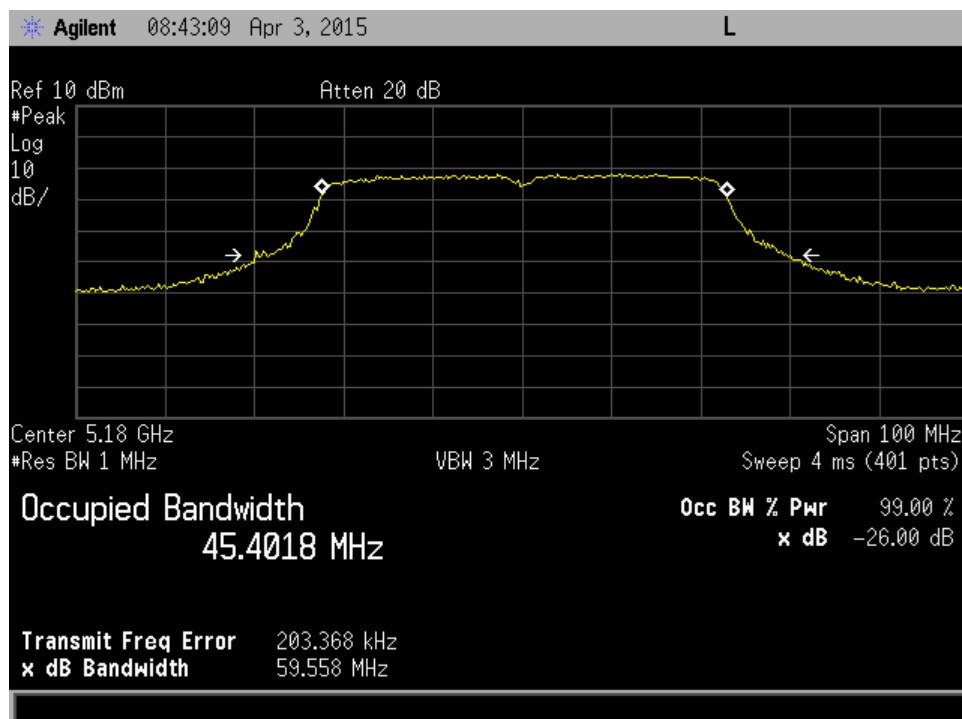
40MHz mid ch J8



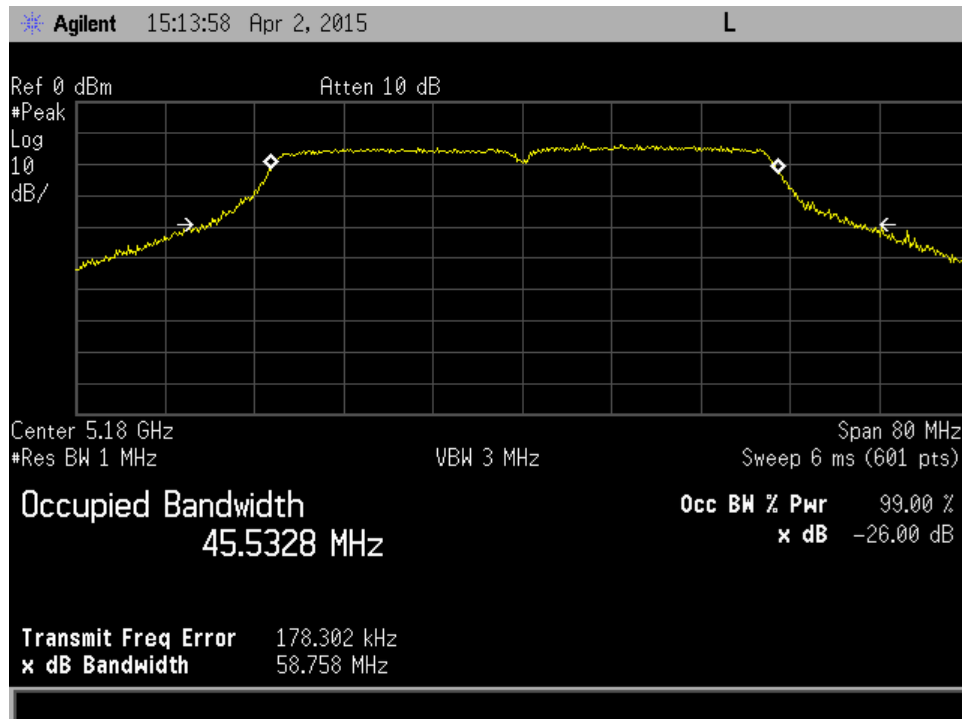
50MHz high ch J7



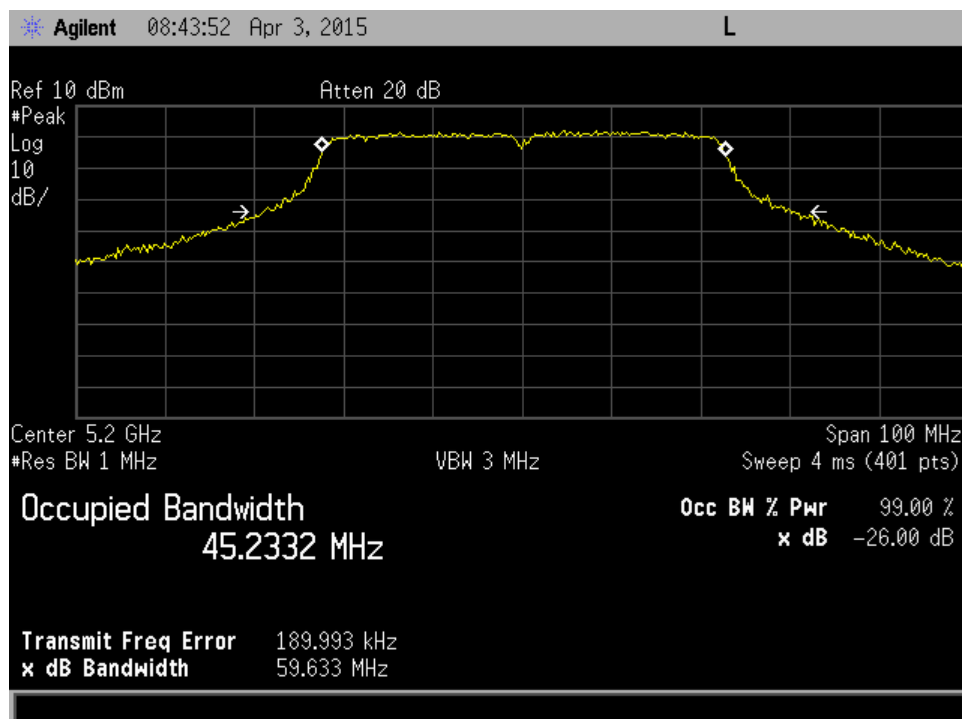
50MHz high ch J8



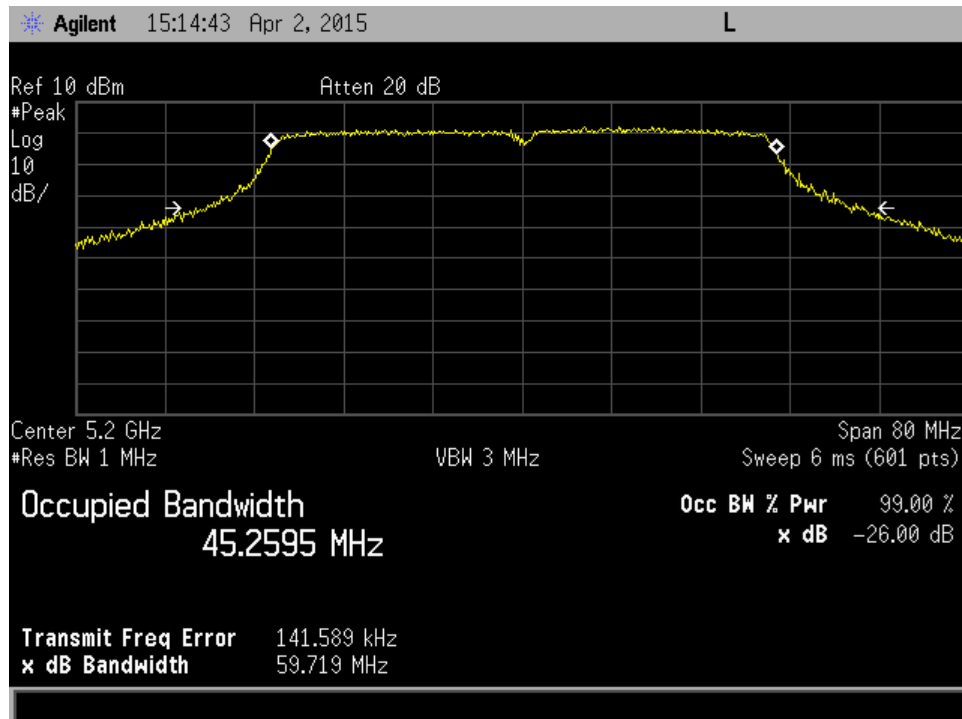
50MHz low ch J7



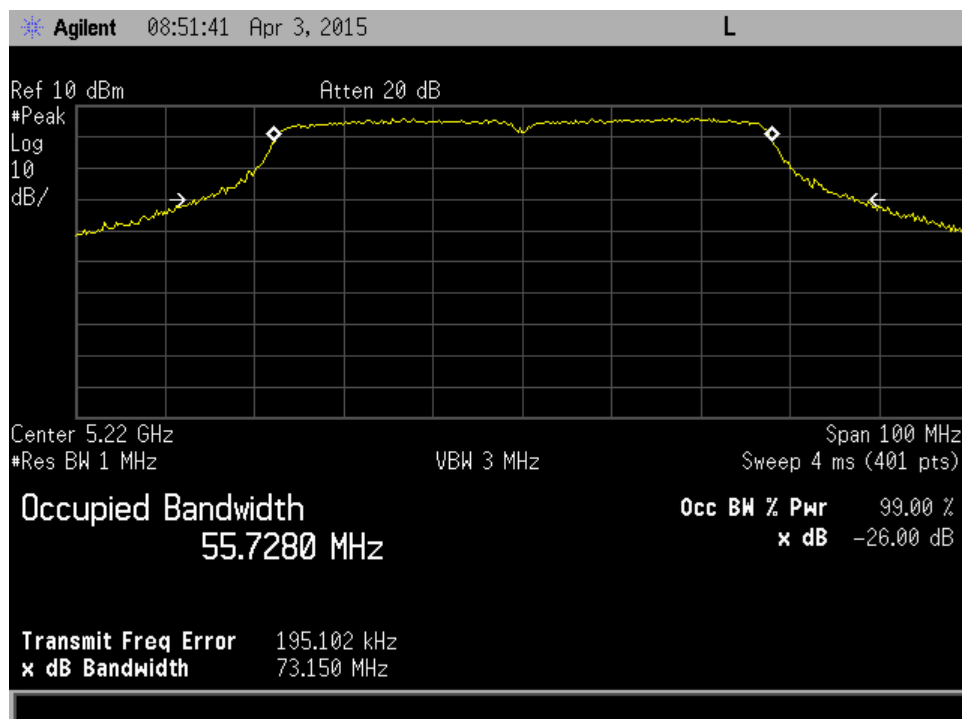
50MHz low ch J8



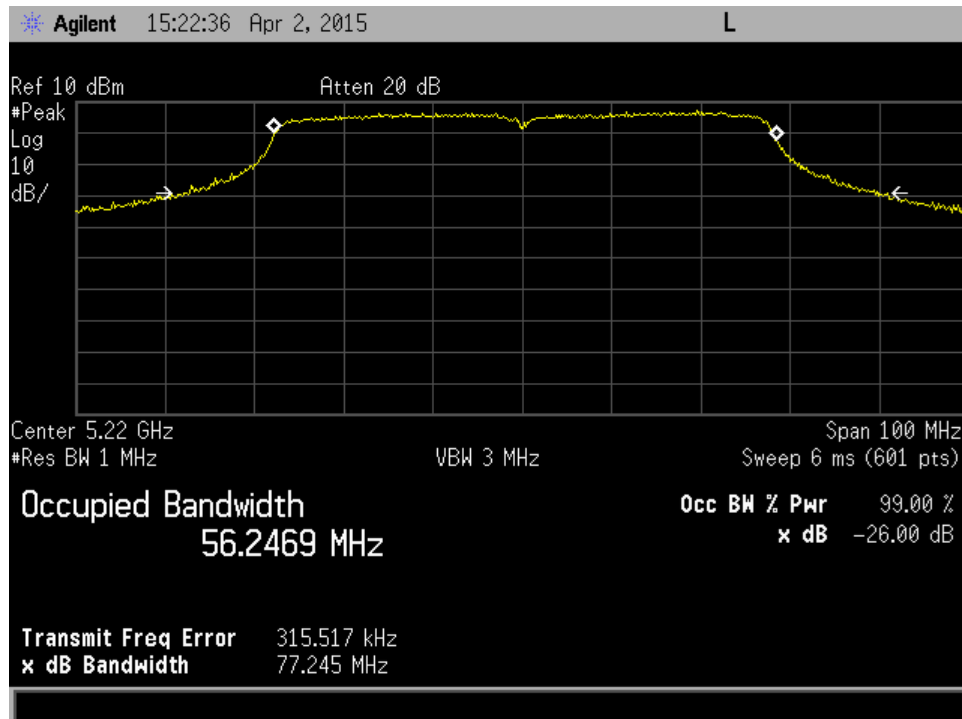
50MHz mid ch J7



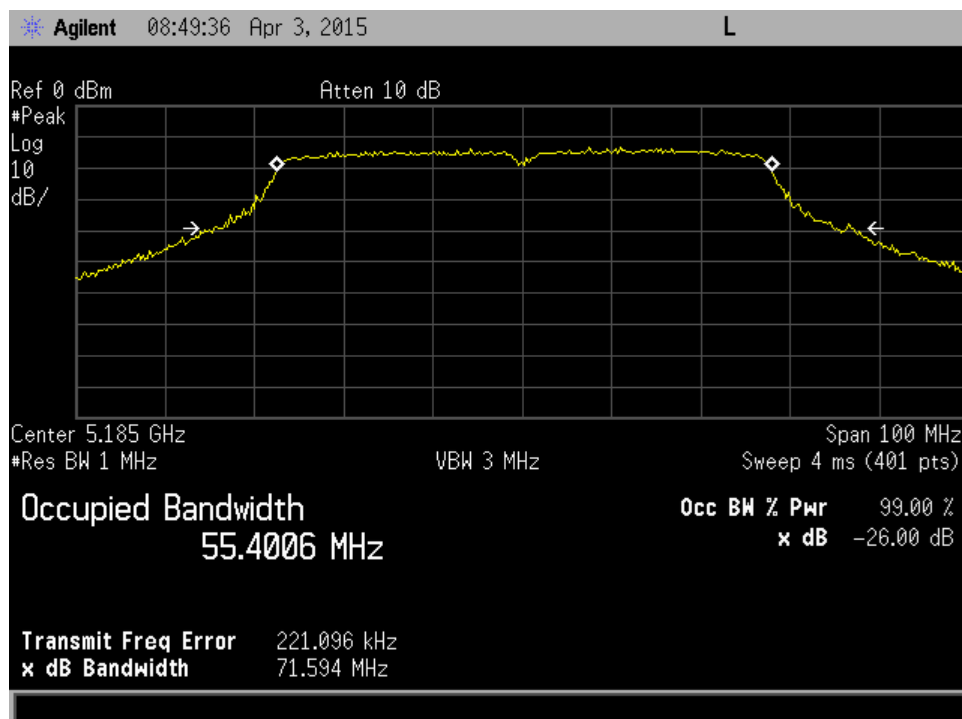
50MHz mid ch J8



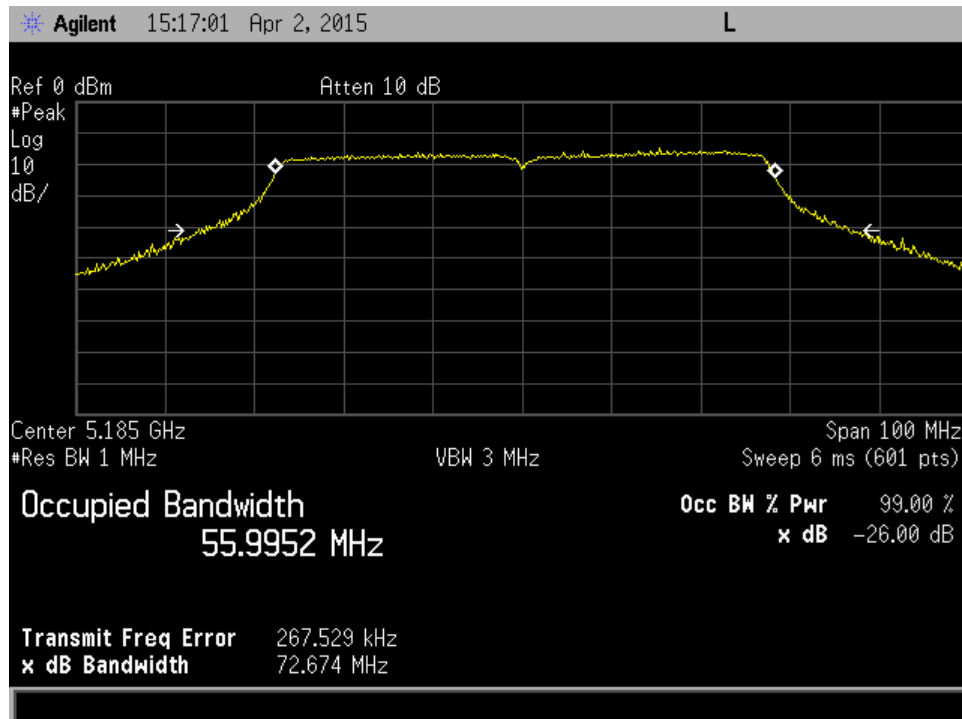
60MHz high ch J7



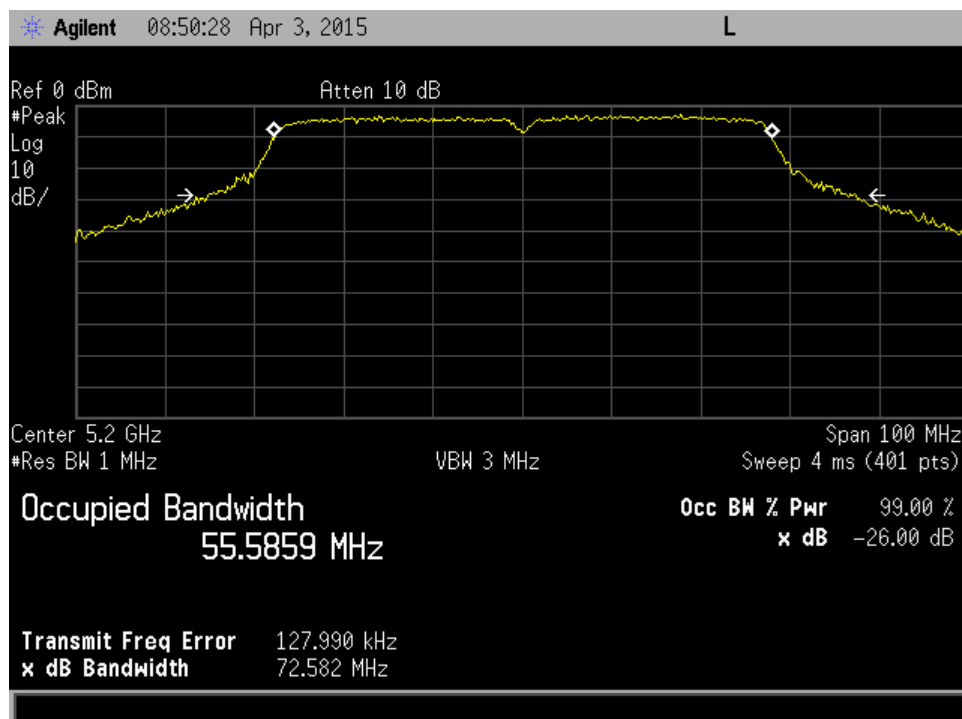
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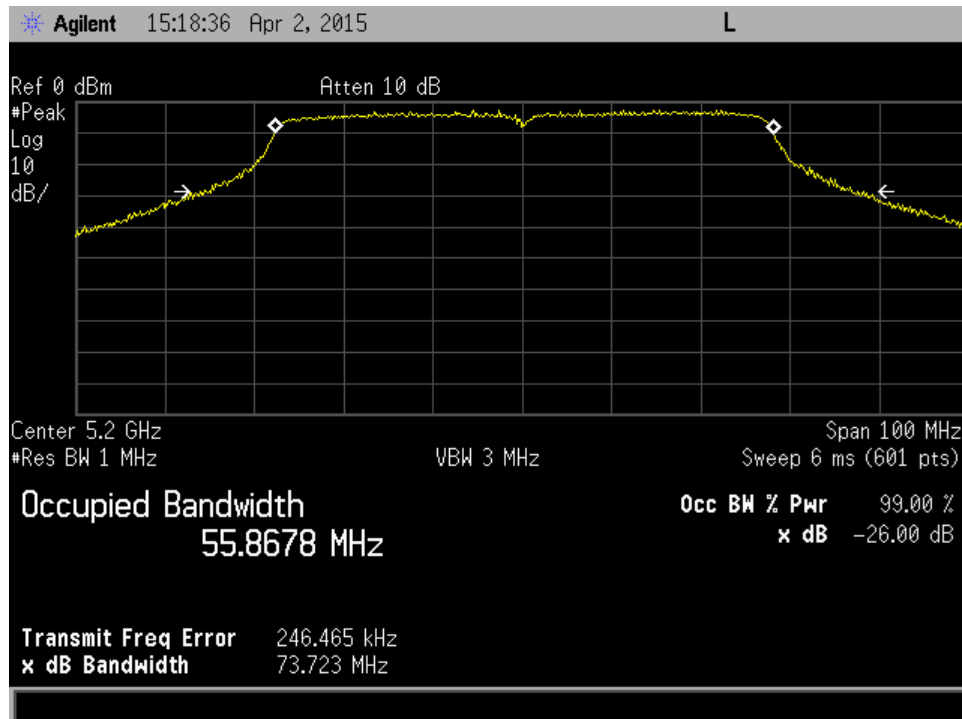
60MHz low ch J7



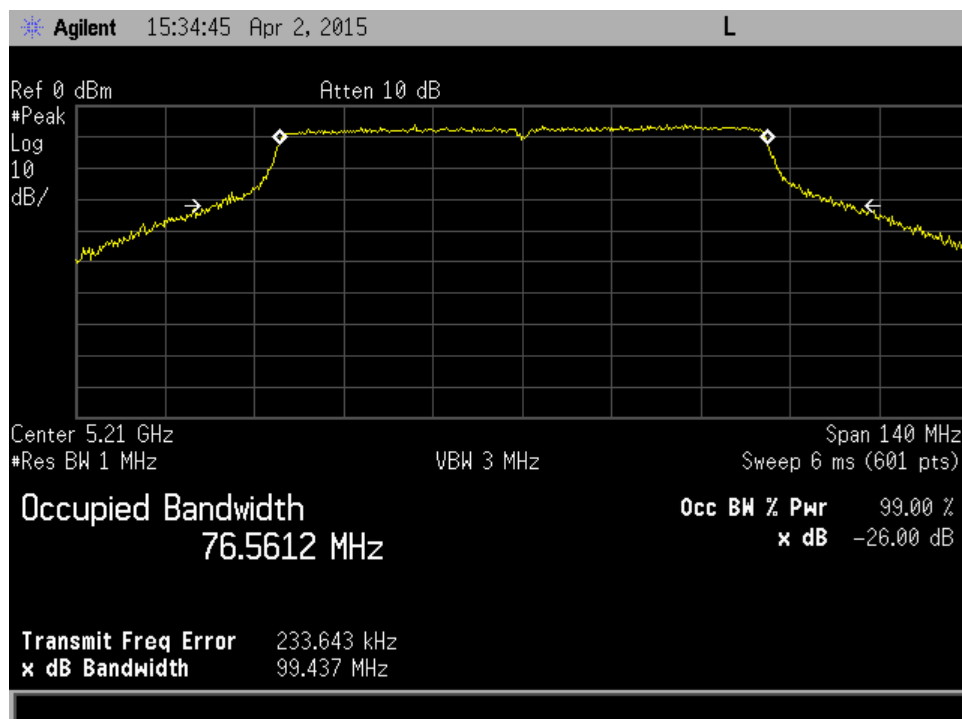
60MHz low ch J8



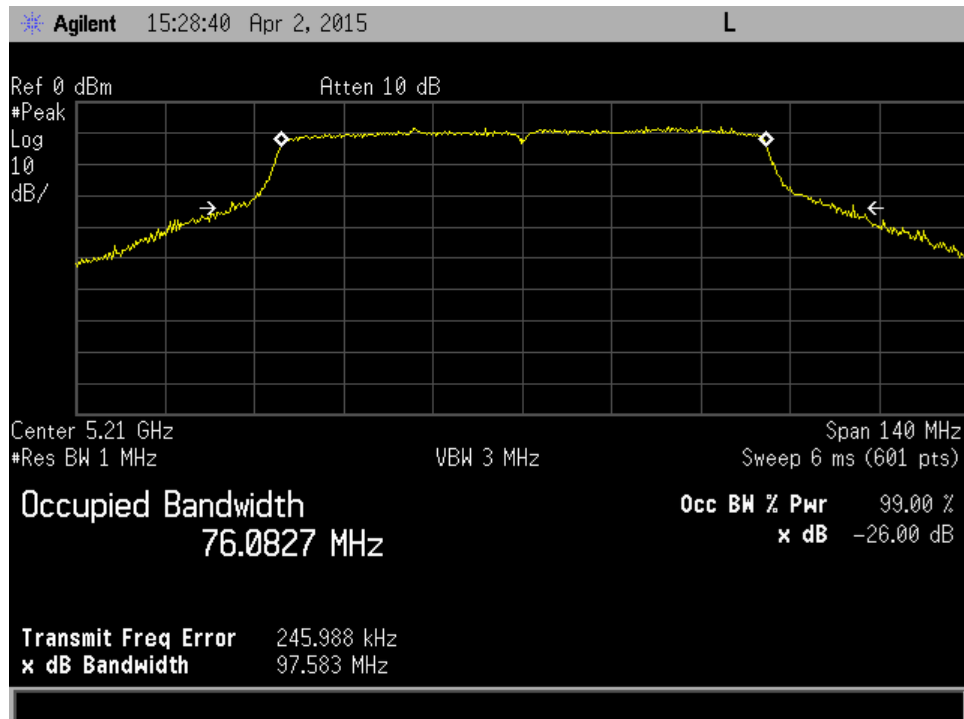
60MHz mid ch J7



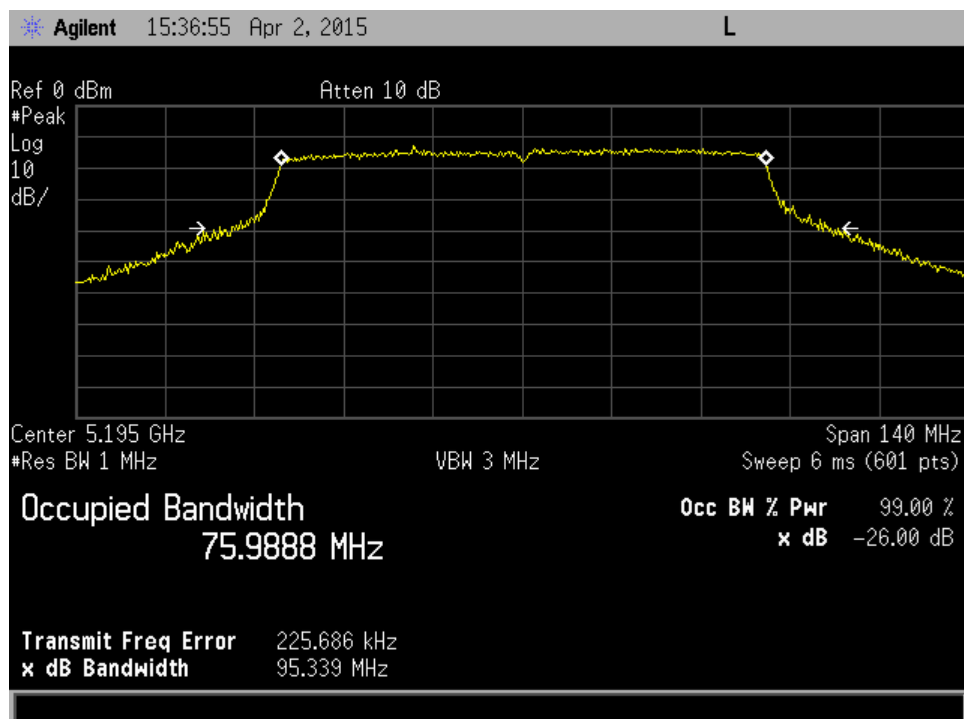
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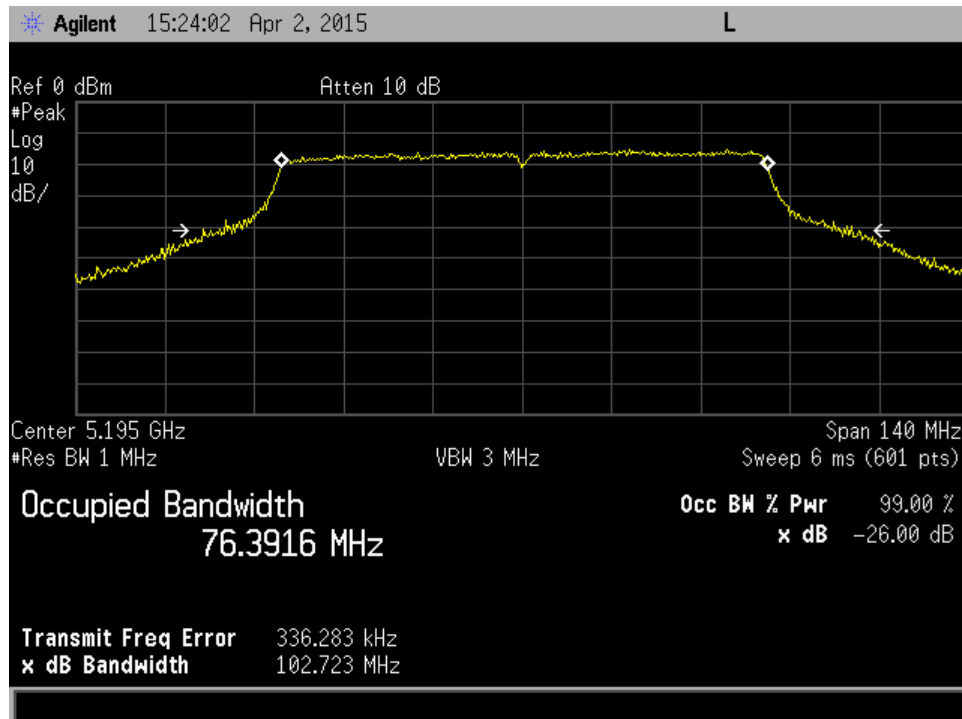
80MHz high ch J7



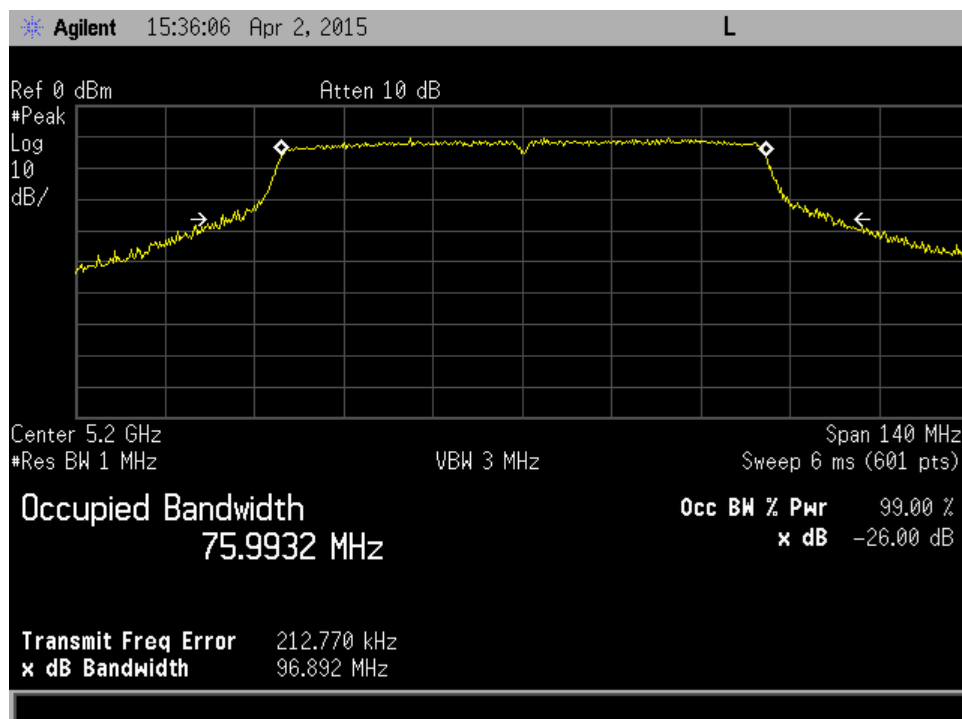
80MHz high ch J8



80MHz low ch J7



80MHz low ch J8



80MHz mid ch J7

